

# Cedar Schematic Beema

2014-03-05

REV : A00

*DY : None Installed*

*UMA: UMA only installed*

*OPS: DISCRTE SG installed*

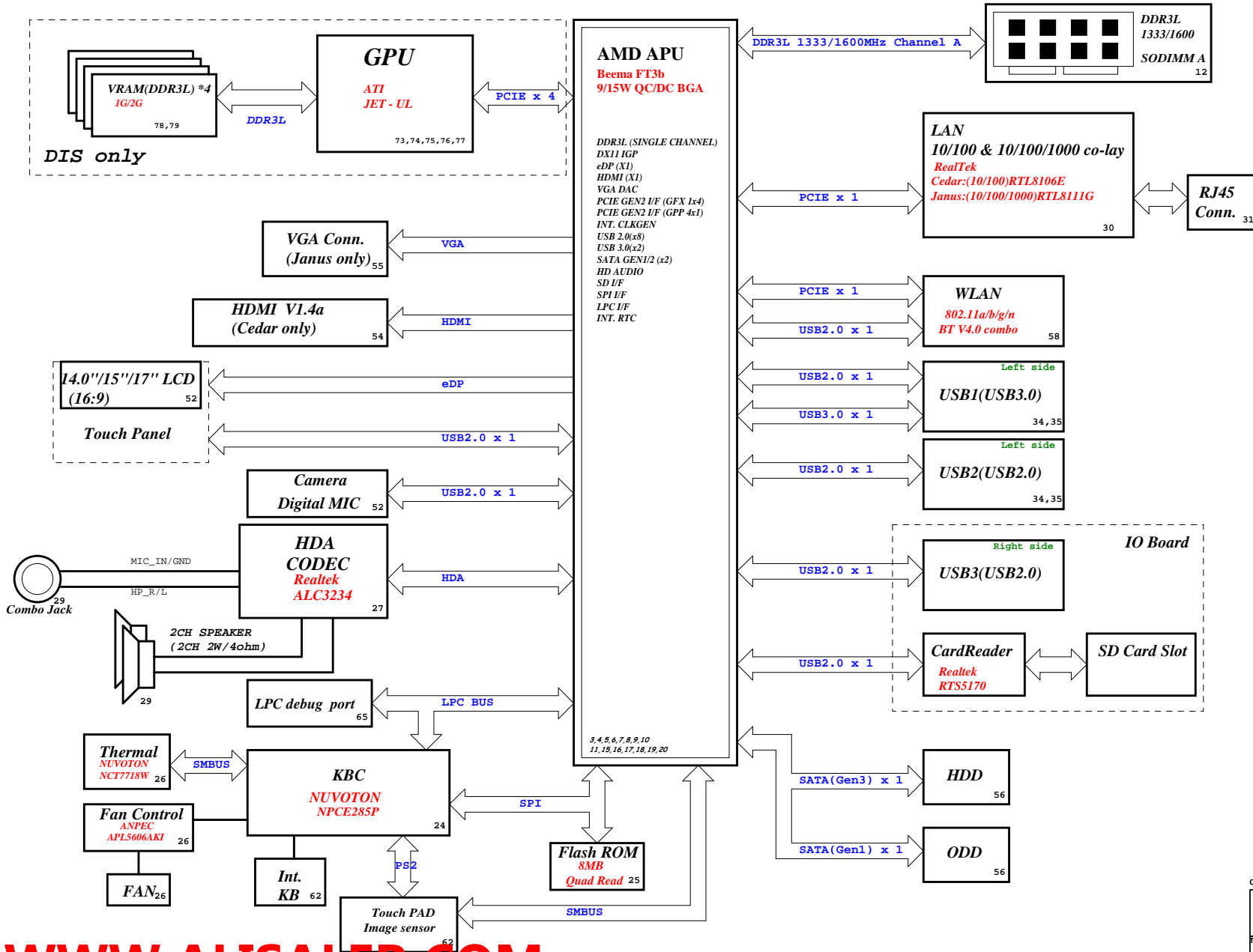
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Cedar UMA 14

<p><b>緯創資通</b> <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</p>	
<p>Title</p>	
<p><b>Cover Page</b></p>	
<p>Size A3</p>	<p>Document Number <b>Cedar AMD BEEMA</b></p>
<p>Date: Wednesday, March 05, 2014</p>	<p>Rev <b>A00</b></p>
<p>Sheet 1 of 104</p>	

Project code:4PD00G010001  
PCB P/N: 13283-1  
Revision: A00

# Cedar Block Diagram

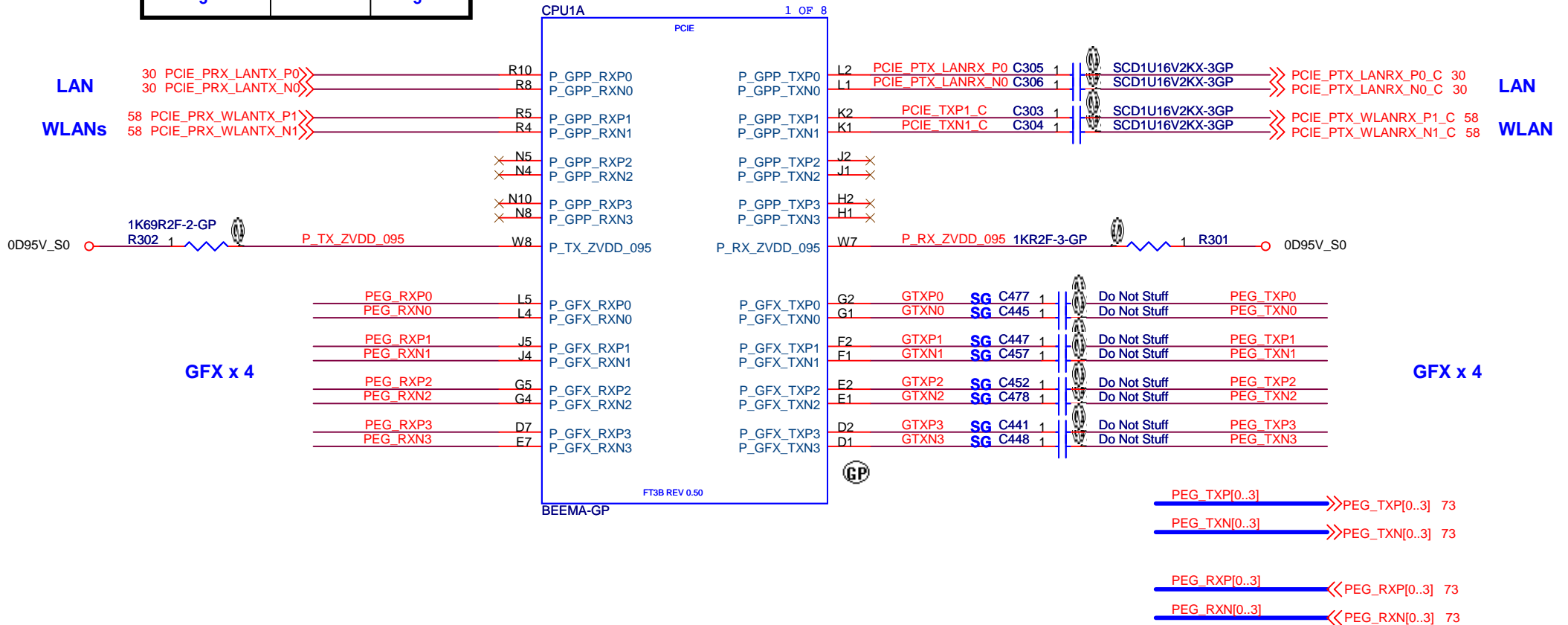


CHARGER	
INPUTS	OUTPUTS
AD+	DCBATOUT
BT+	
SYSTEM DC/DC	
TPS51225RUKR-GP 45	
INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 5V_AUX_S5 5V_S5 3D3V_S5
CPU Core Power	
ISL95813HRZ-GP 46,47	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
DDR3L SUS	
TPS51716RUKR-GP 49	
INPUTS	OUTPUTS
DCBATOUT	1D35V_S3 0D65V_S0
CPU 1.05V	
RT8237CZQW-2-GP 48	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0
VDDIO_AZ	
TLV70215DBVR 36	
INPUTS	OUTPUTS
3D3V_S5	1D5V_S0
Switches 36 83	
INPUTS	OUTPUTS
1D35V_S3	1D35V_S0
5V_S5	5V_S0
3D3V_S5	3D3V_S0
0D95V_S5	0D95V_VGA_S0
3D3V_S0	3D3V_VGA_S0
1D35V_S3	1D35V_VGA_S0
1D8V_S5	1D8V_VGA_S0
PCB LAYER	
L1:TOP L2:VCC L3:Signal L4:Signal L5:GND L6:BOT	

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File Block Diagram	
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GPP CLK port	Device	CLKREQ#
0	LAN WLAN	0
1		1
2		2
3		3



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Title

**CPU (PCIE)**

Size  
A4

Document Number

**Cedar AMD BEEMA**

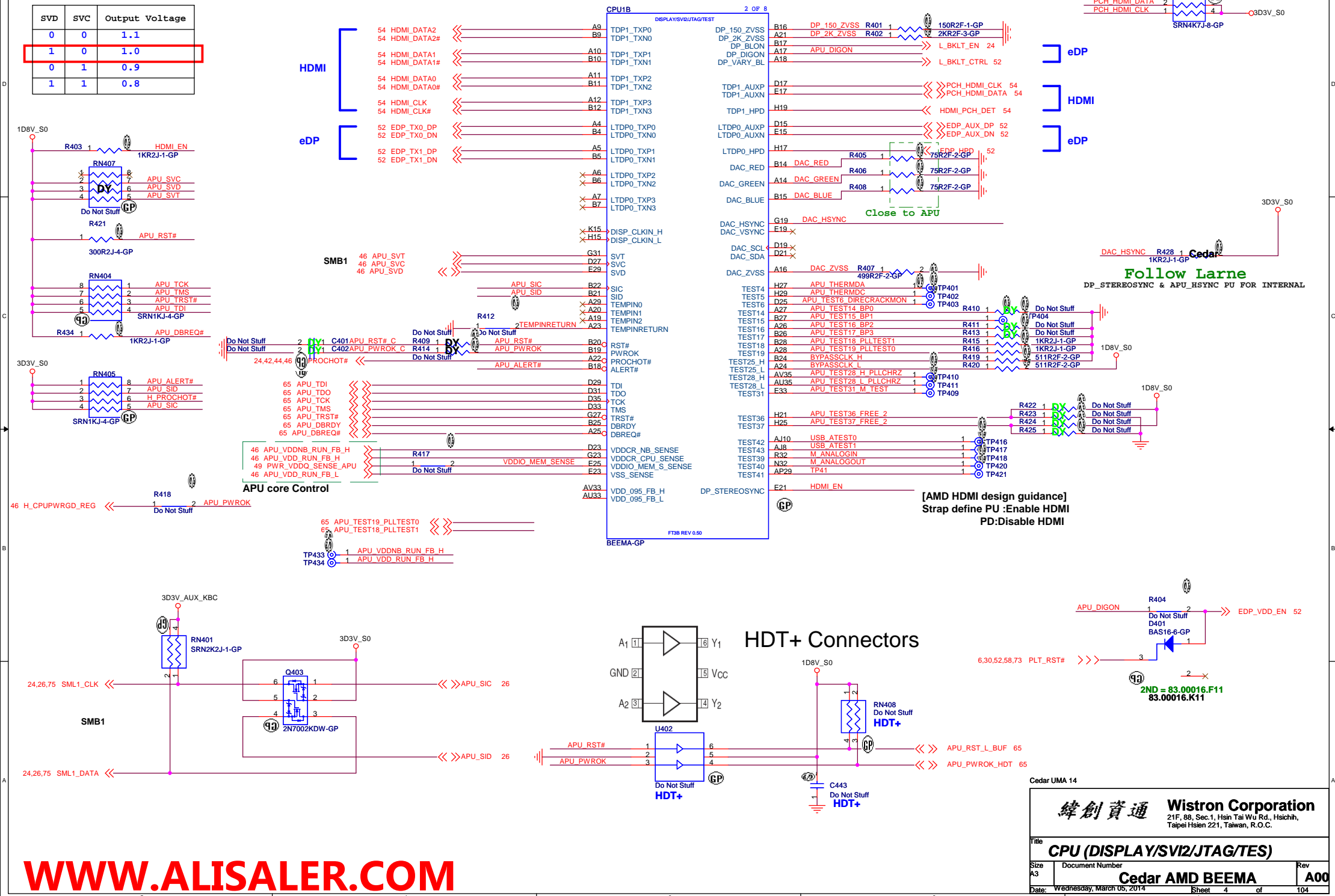
Rev  
A00

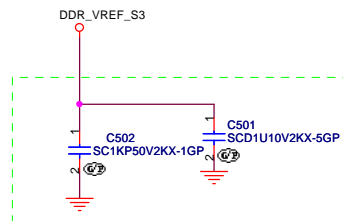
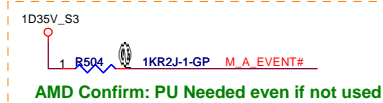
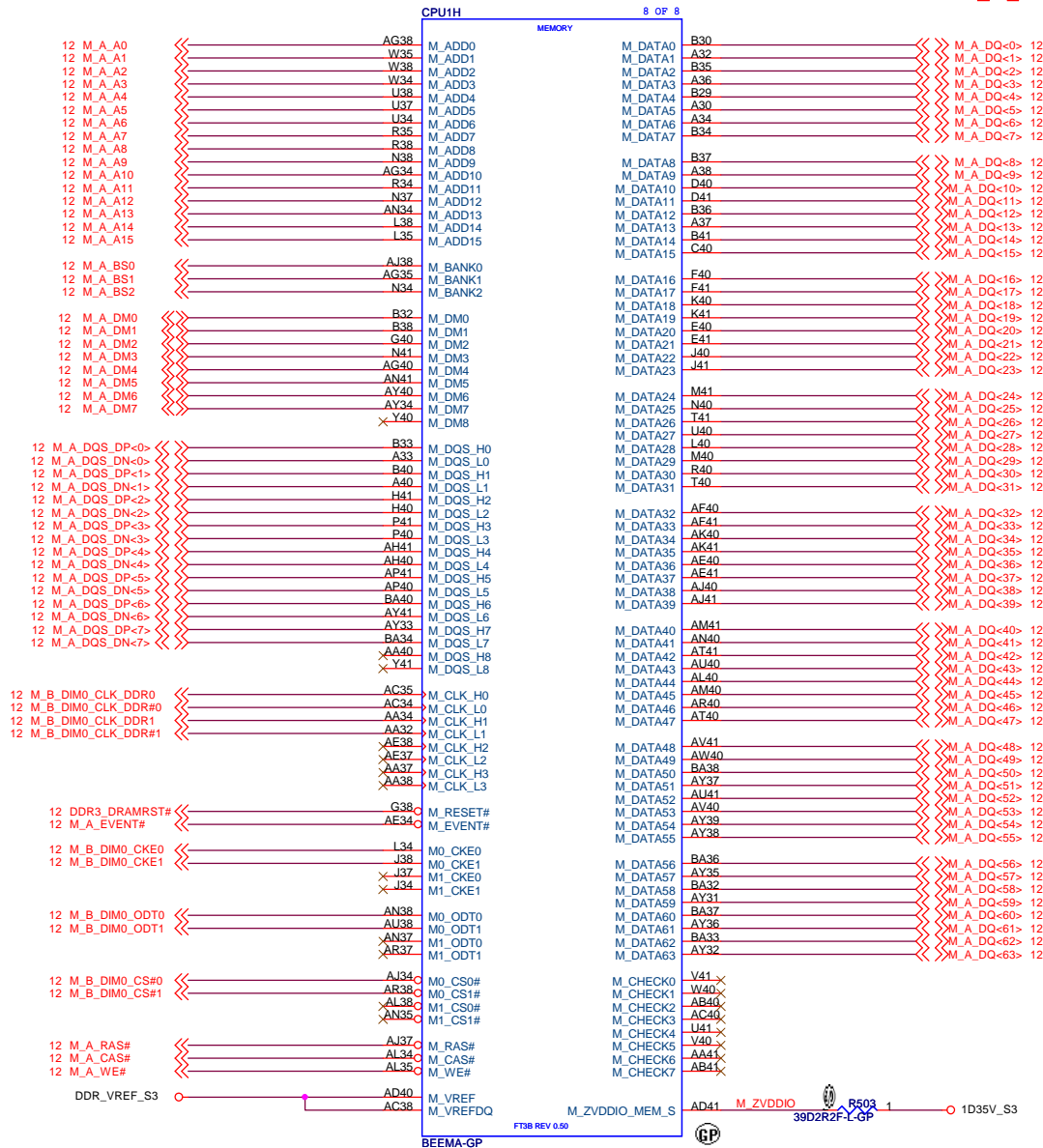
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### Pre-PWROK METAL VID CODES

SVD	SVC	Output Voltage
0	0	1.1
1	0	1.0
0	1	0.9
1	1	0.8



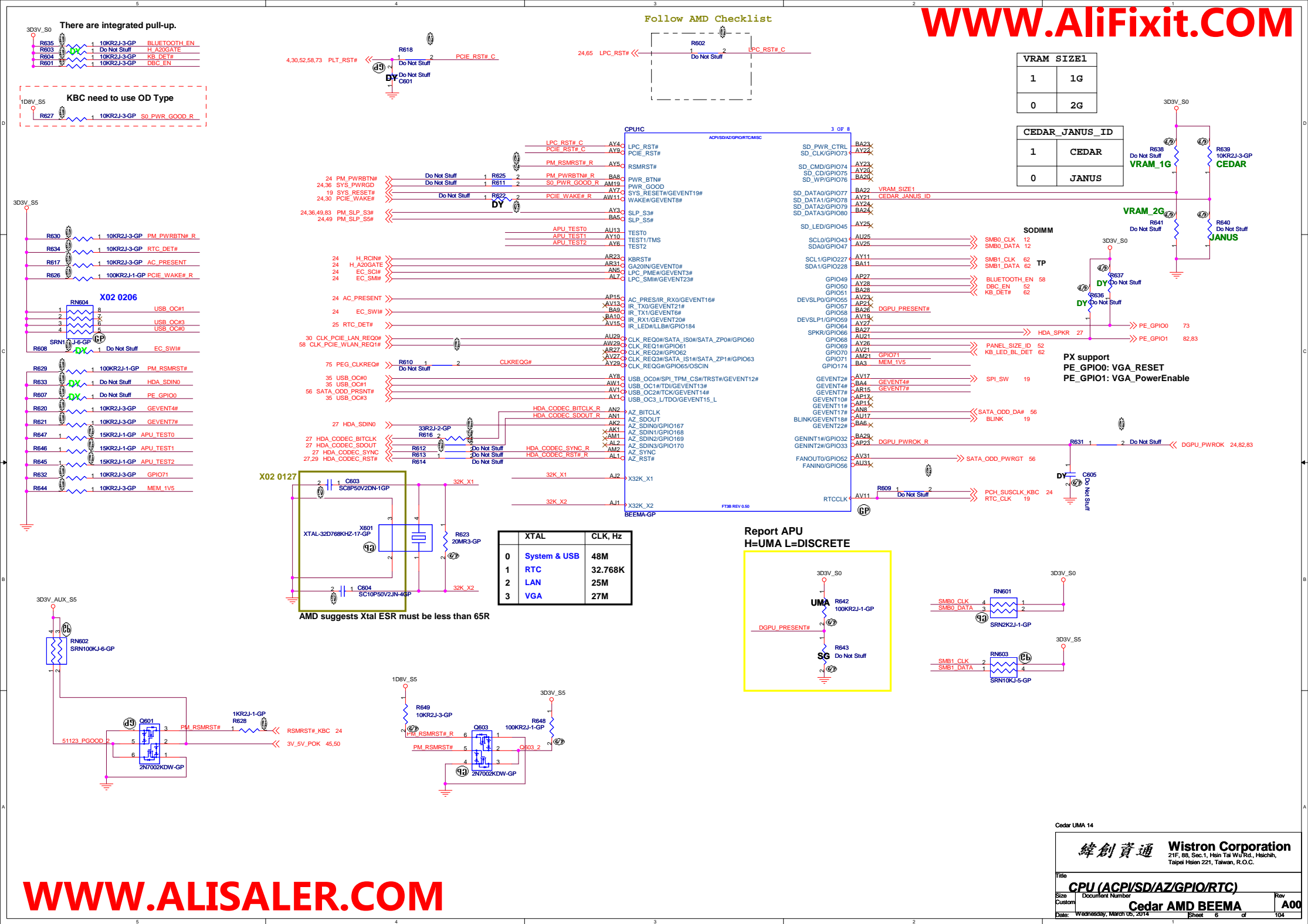


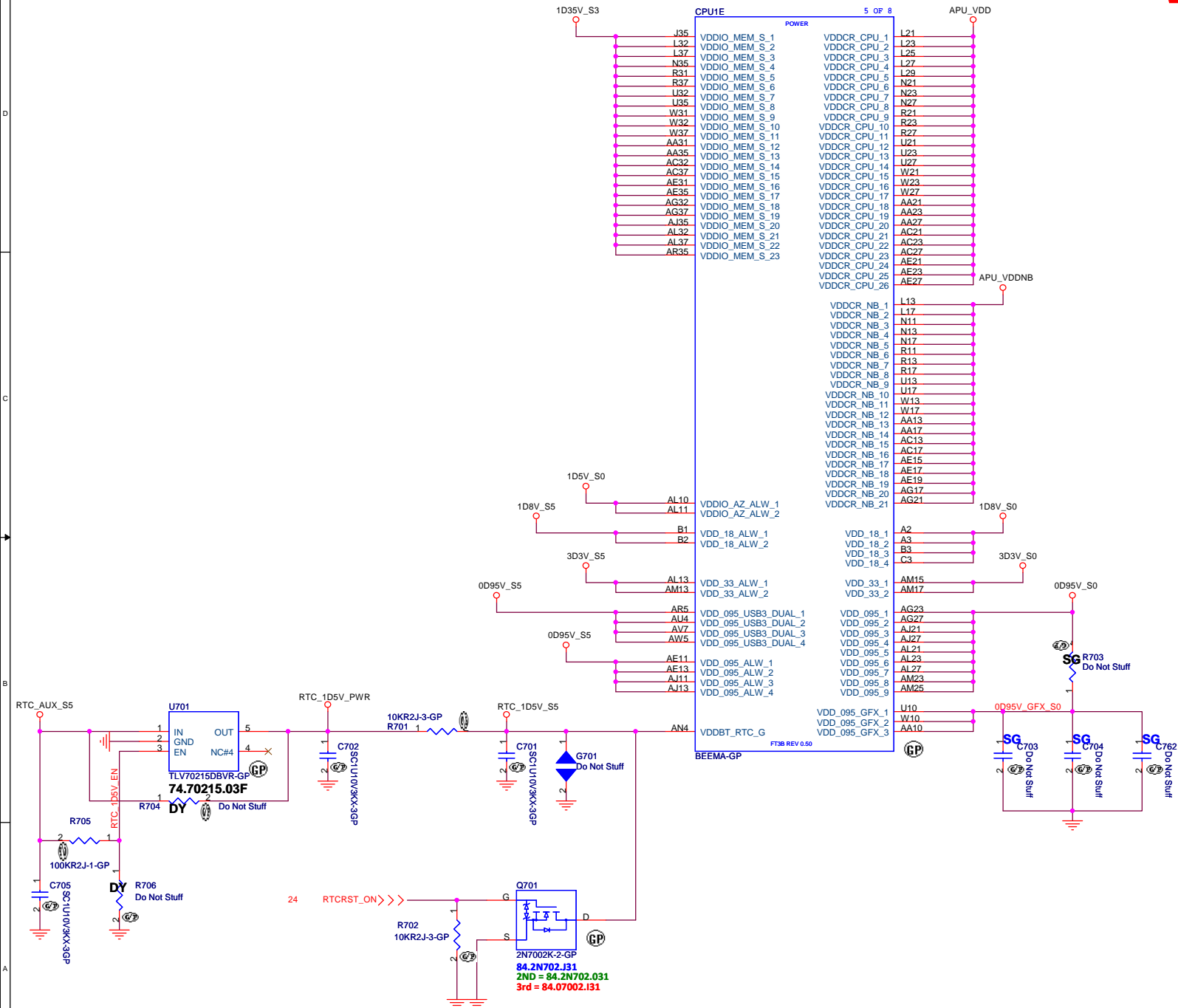
LAYOUT: place them close to APU

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Title		
<b>CPU (ACPI/SD/AZ/GPIO/RTC)</b>		
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	XTAL	CLK, Hz
0	System & USB	48M
1	RTC	32.768K
2	LAN	25M
3	VGA	27M





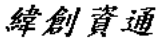
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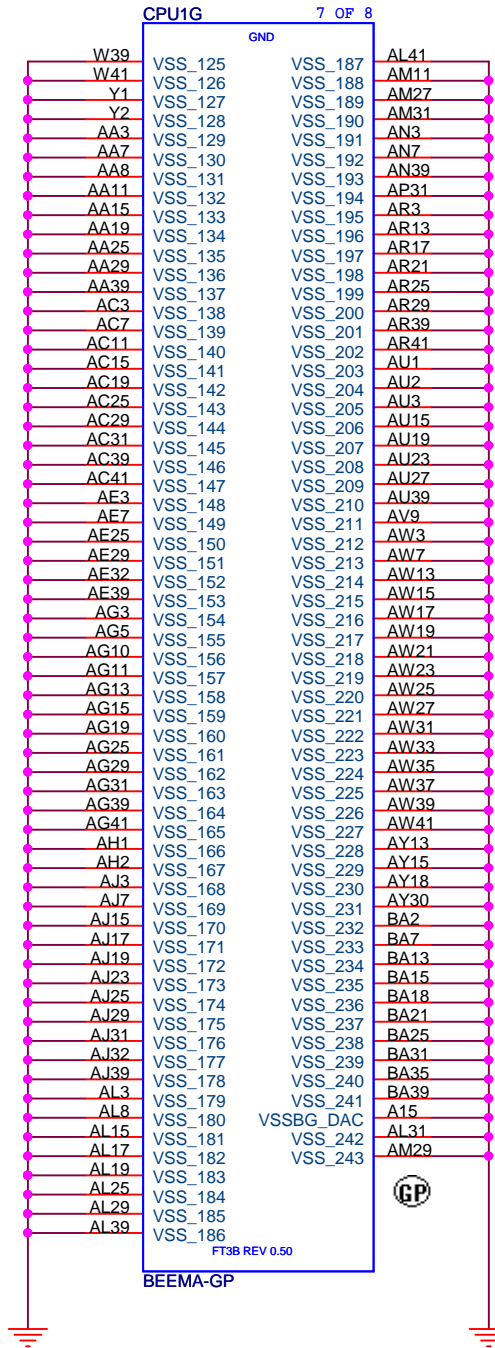
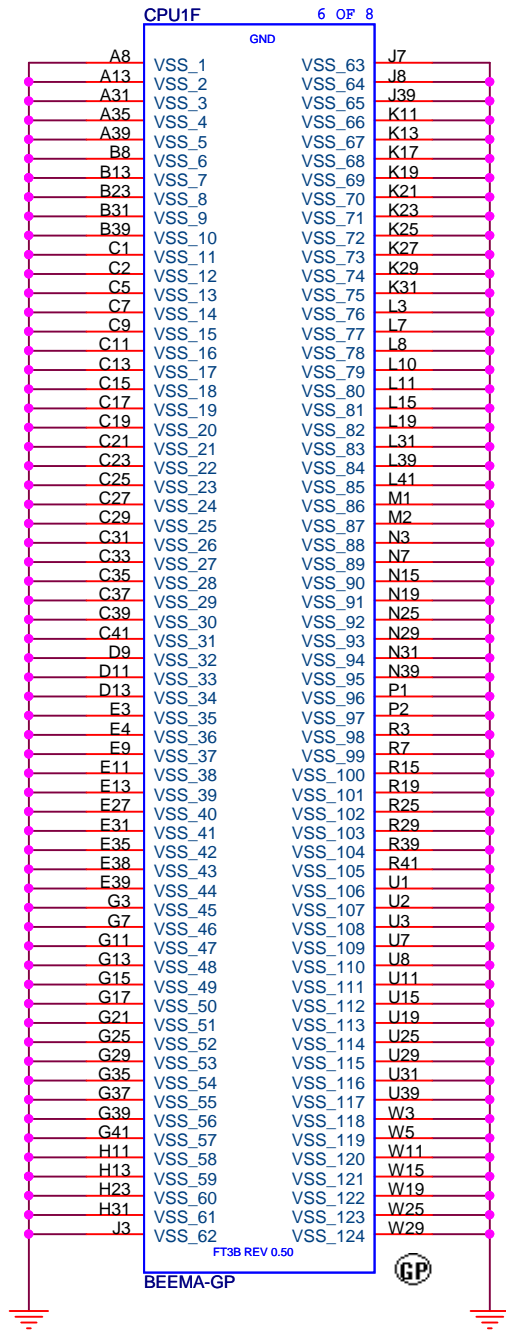
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Size	Document Number	Rev		
A3		<b>Cedar AMD BEEMA</b>		<b>A00</b>
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Title

**CPU (VSS)**

Size  
A4

Document Number

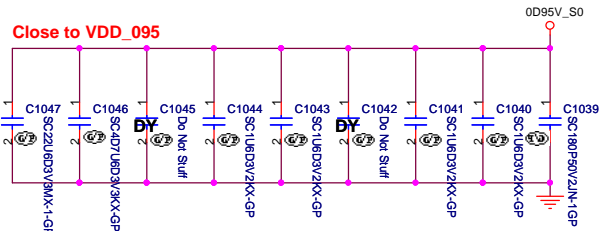
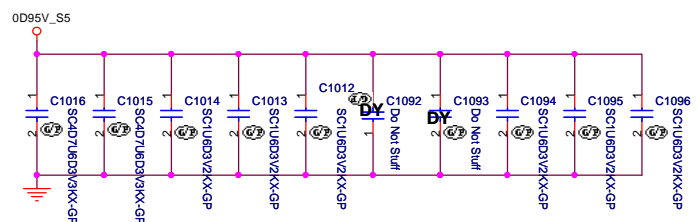
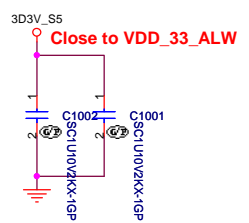
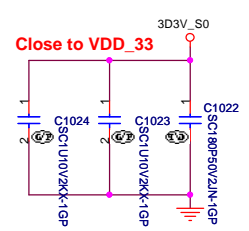
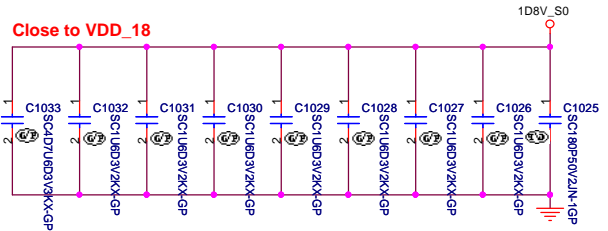
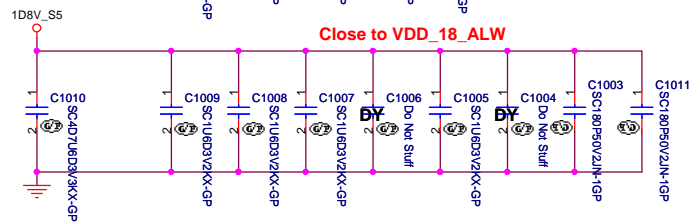
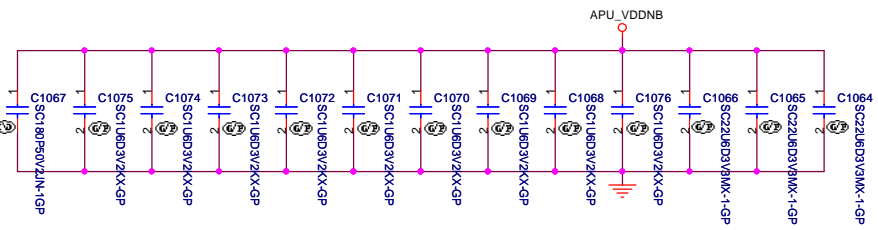
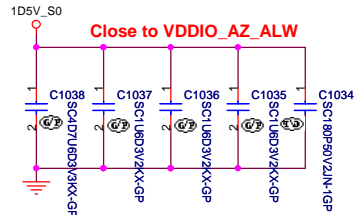
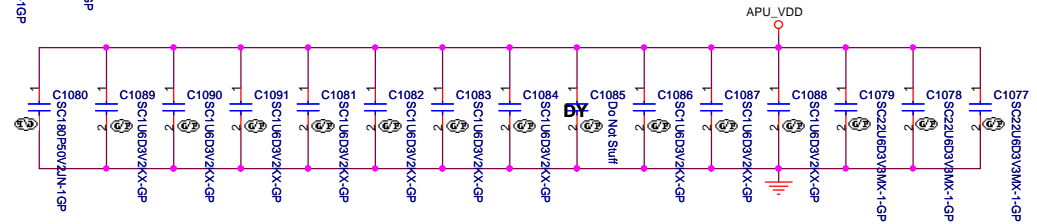
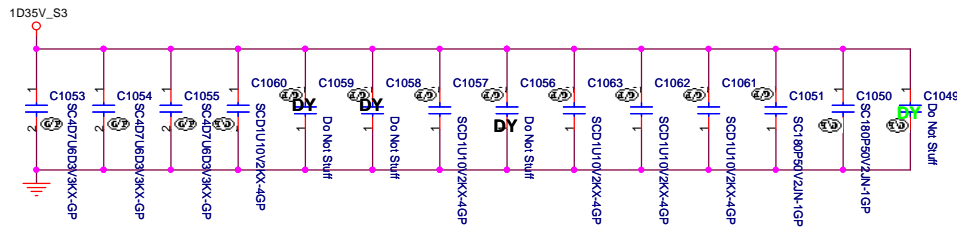
**Cedar AMD BEEMA**

Rev

**A00**

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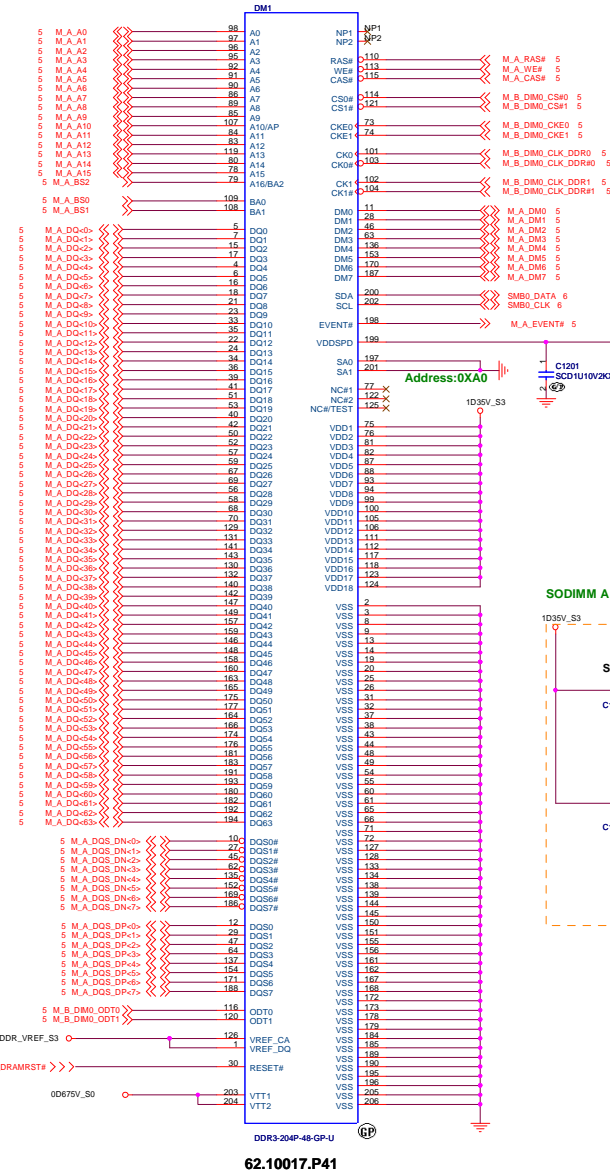


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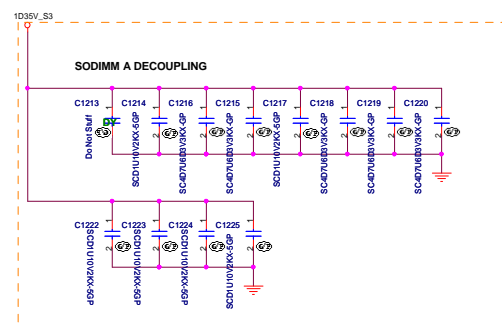
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SSID = MEMORY



SODIMM A DECOUPLING

Layout Note: Place these Caps near SO-DIMMA.



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Title <div>DDR3-SODIMM2</div>		
Size <div>A4</div>	Document Number <div>Cedar AMD BEEMA</div>	Rev <div>A00</div>
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Title <div>Reserved</div>		
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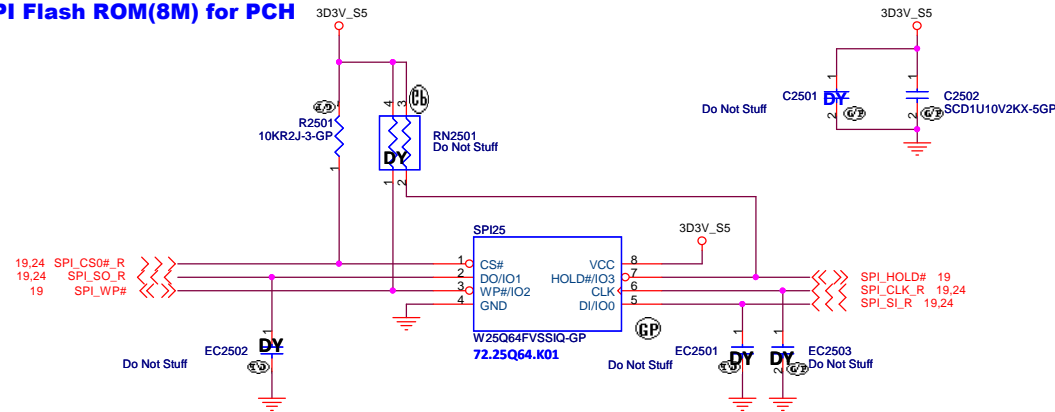
**KBC Nuvoton NPCE885**

<div style="text-align: center;"> <b>KBC Nuvoton NPCE885</b> </div>			
Size	Document Number		Rev
Custom	<div style="text-align: center;"> <b>Cedar AMD BEEMA</b> </div>		<div style="text-align: center;"> <b>A00</b> </div>
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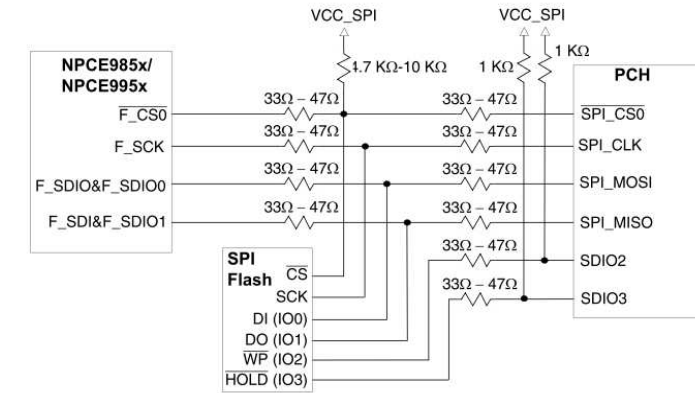
SSID = Flash.ROM

### SPI Flash ROM(8M) for PCH



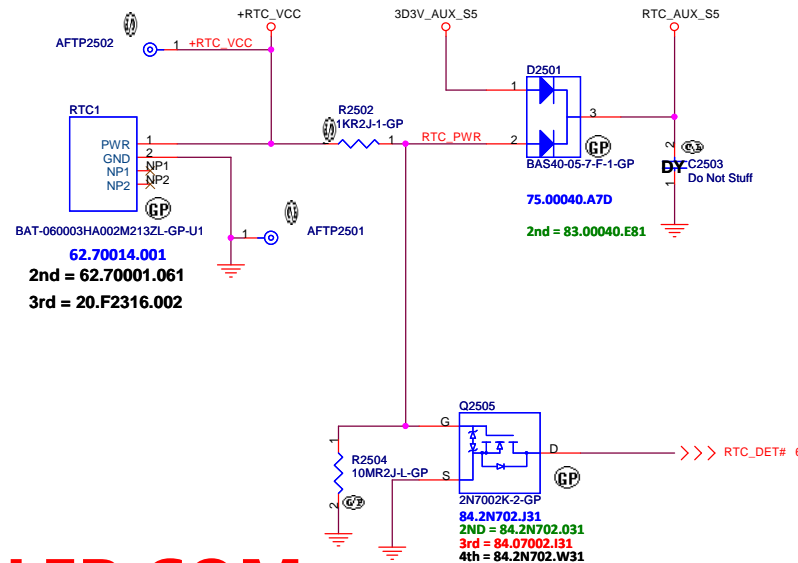
Source	QUAD/DUAL fast read	DUAL fast read
72.25Q64.K01	o	o
72.25647.00A	o	o

### Single SPI shared flash connection (SPI Quad I/O mode)



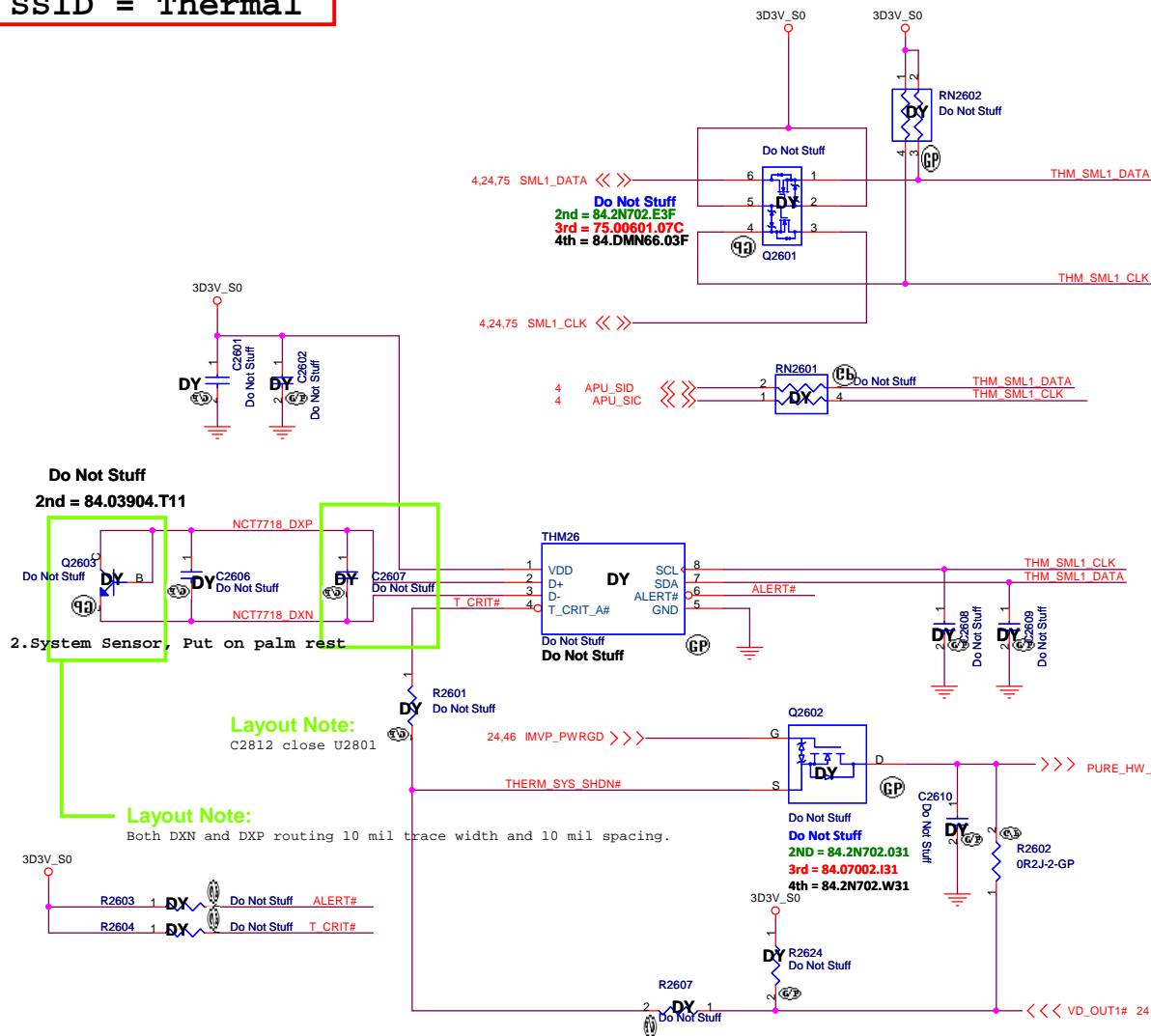
Refer to "NPCE985x/ NPCE995x board design reference guide"

SSID = RBATT



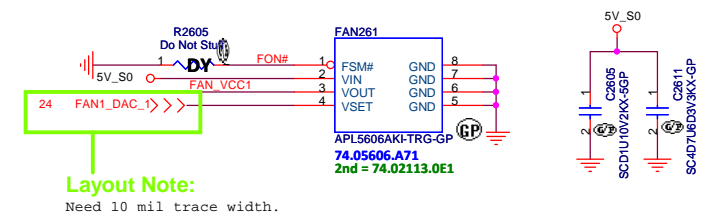
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SSID = Thermal



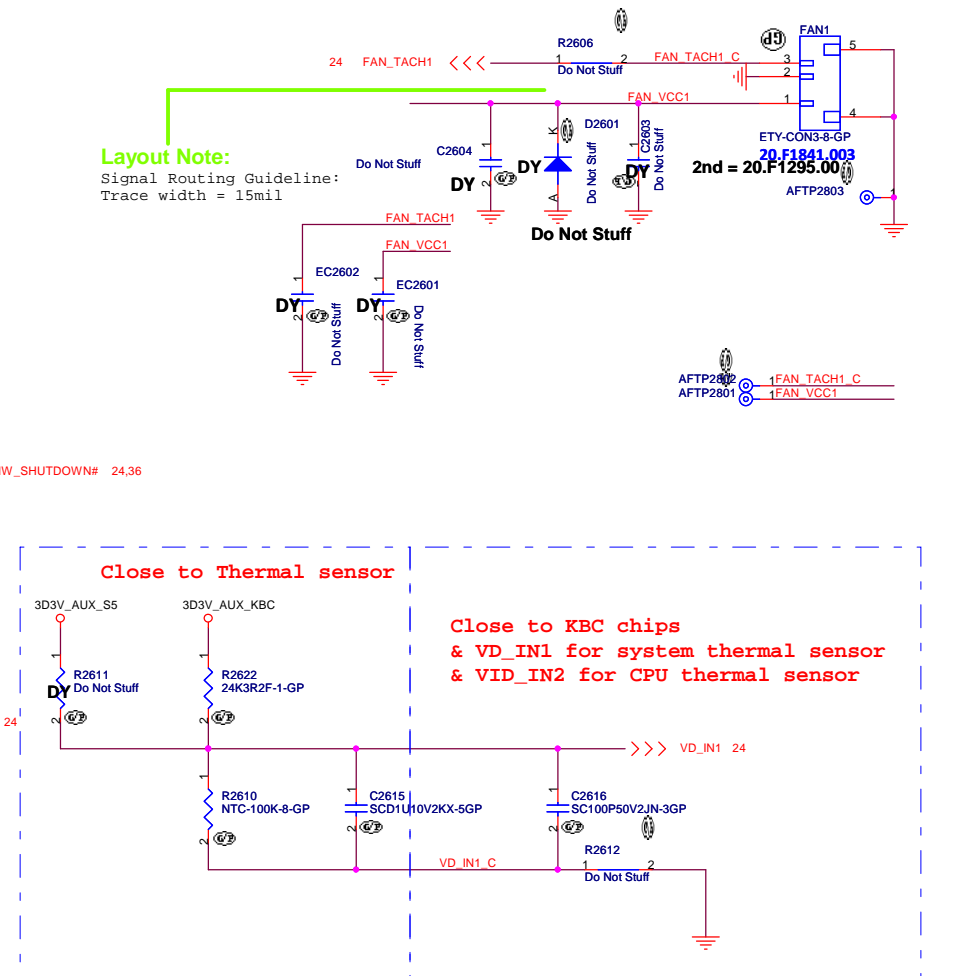
TEMPERATURE (°C)	T_CRIT#				
	2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107
	7.5KΩ	79	89	99	109
	10.5KΩ	81	91	101	111
	14KΩ	83	93	103	113
	18.7KΩ	85	95	105	115

### Fan controller1



### Layout Note:

Signal Routing Guideline:  
Trace width = 15mil



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Title	THERMAL NCT7718W/Fan		
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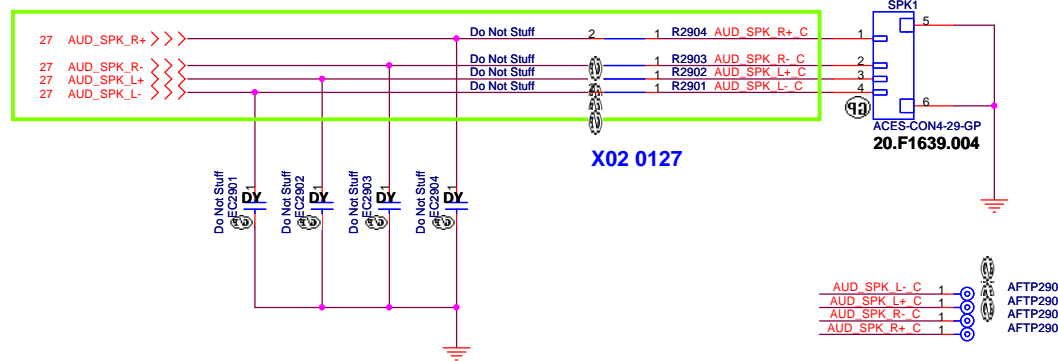
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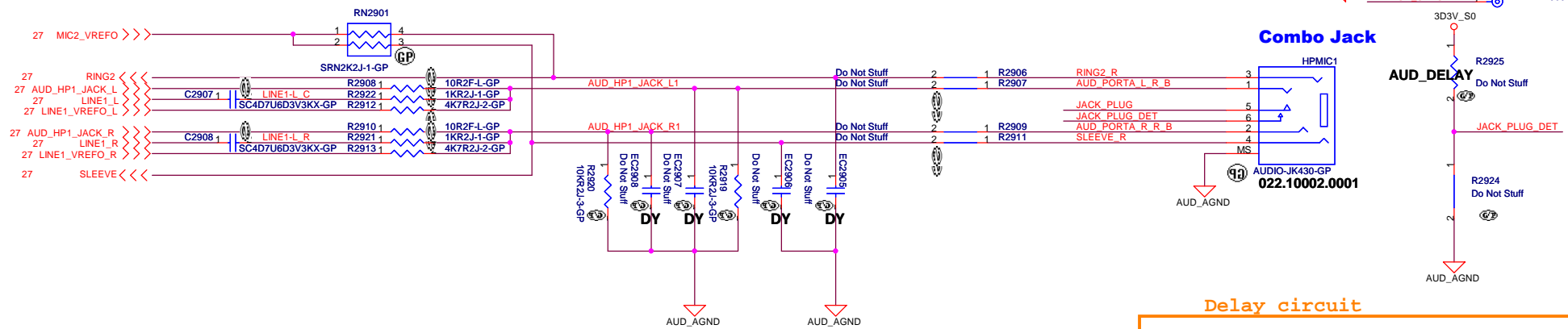
## Layout Note:

Speaker trace width &gt;40mil @ 2W4ohm speaker power

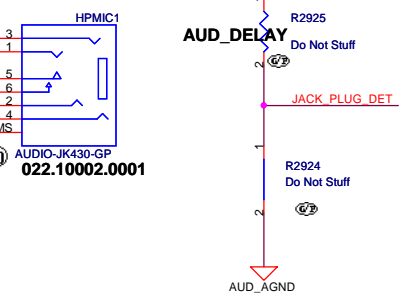


CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L-

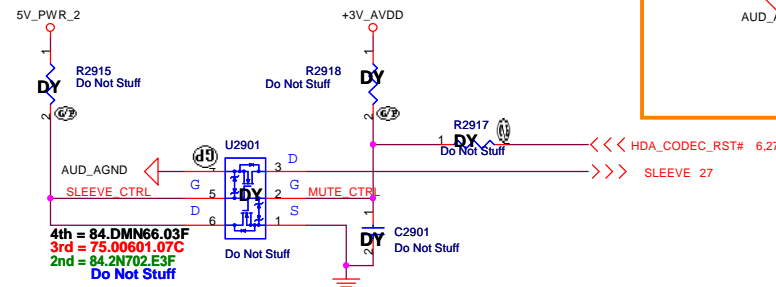
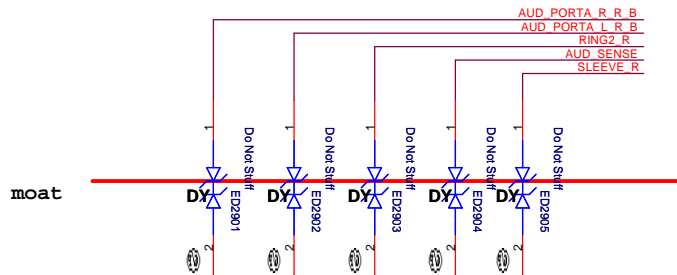
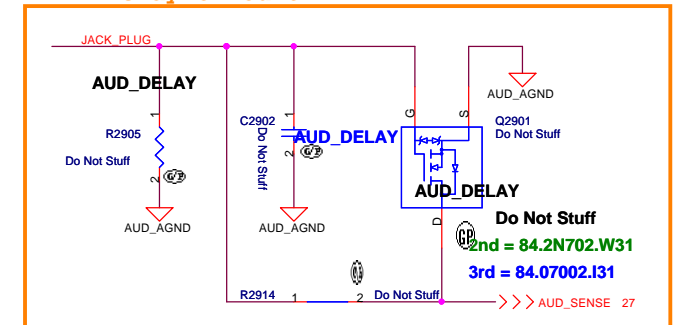
AUD\_SPK\_L- C 1 AFTP2901  
 AUD\_SPK\_L+ C 1 AFTP2902  
 AUD\_SPK\_R- C 1 AFTP2903  
 AUD\_SPK\_R+ C 1 AFTP2904



## Combo Jack



## Delay circuit

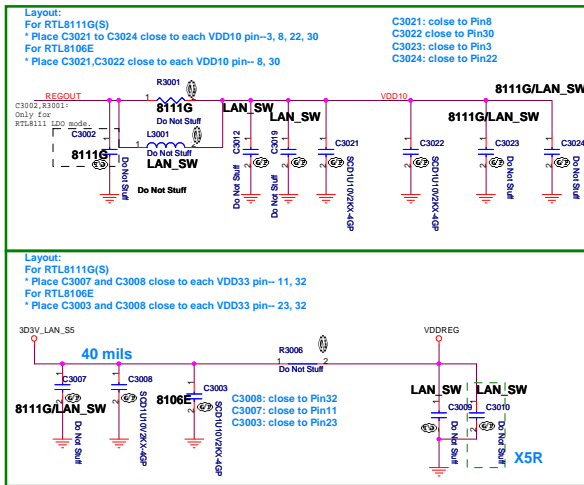


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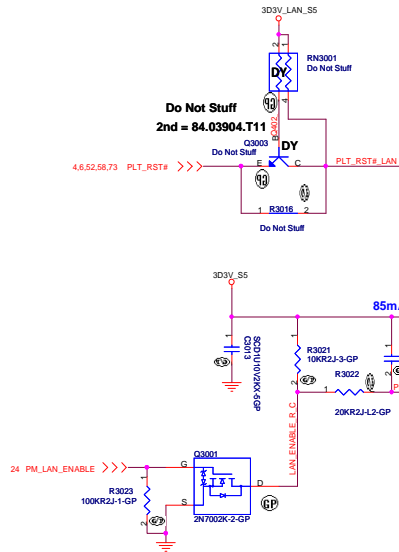
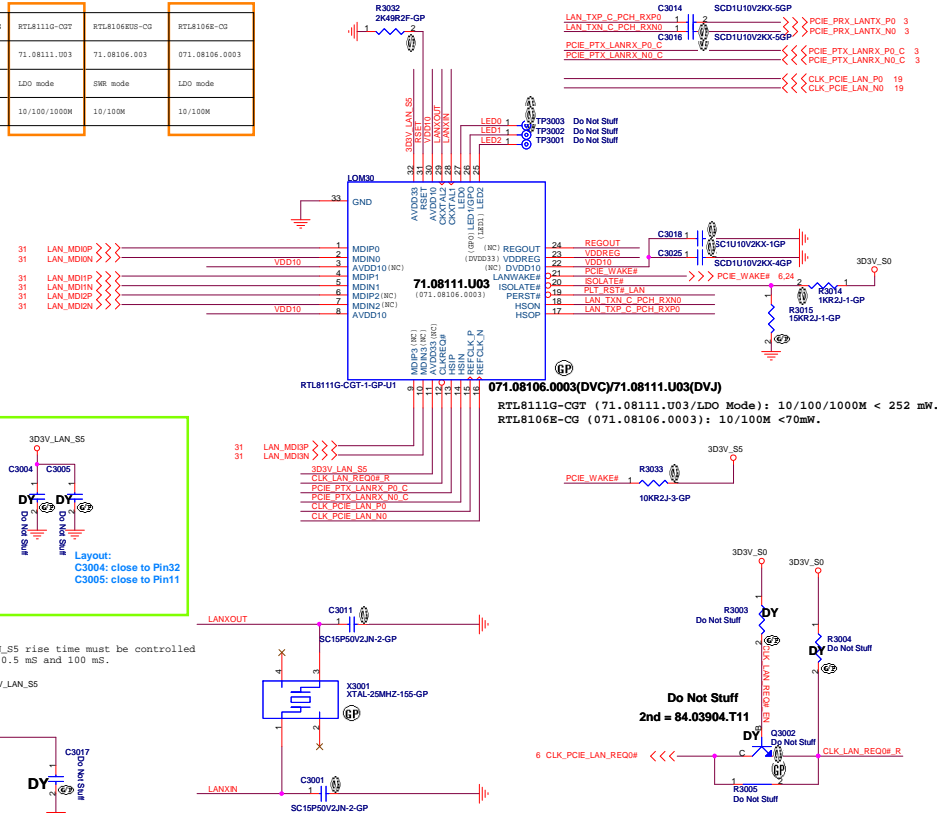
Title Thermal NCT7718W/Fan Controller P2793

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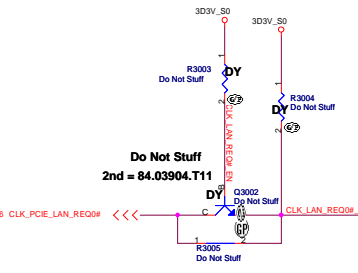
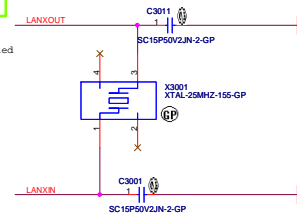


**LAN CHIP (10/100/1000M & 10/100M co-lay)**

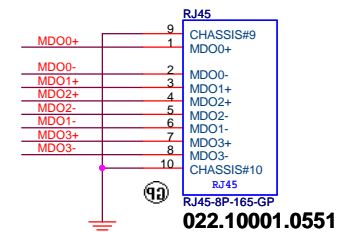
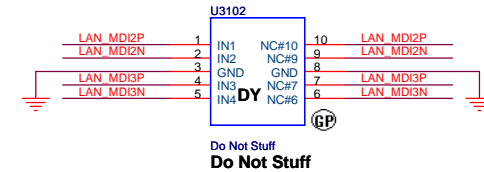
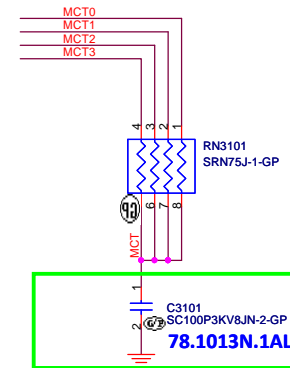
RTL8111GUS-CG	RTL8111G-DT	RTL8106EUS-CG	RTL8106E-CG
71.08111.W03	71.08111.U03	71.08106.U03	071.08106.0003
SWR mode	LDO mode	SWR mode	LDO mode
10/100/1000M	10/100/1000M	10/100M	10/100M



3D3V\_LAN\_S5 rise time must be controlled between 0.5 mS and 100 mS.

[illegible]

Layout note:  
30 mil spacing between MDI differential pairs.



AFTP3107	1	MDO0+
AFTP3102	1	MDO0-
AFTP3101	1	MDO1+
AFTP3103	1	MDO2+
AFTP3104	1	MDO2-
AFTP3106	1	MDO1-
AFTP3105	1	MDO3+
AFTP3108	1	MDO3-

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Title <div>(Reserved)Card Reader</div>		
Size <div>A4</div>	Document Number <div>Cedar AMD BEEMA</div>	Rev <div>A00</div>
Date: Wednesday, March 05, 2014		Sheet 32 of 104



( Blanking )

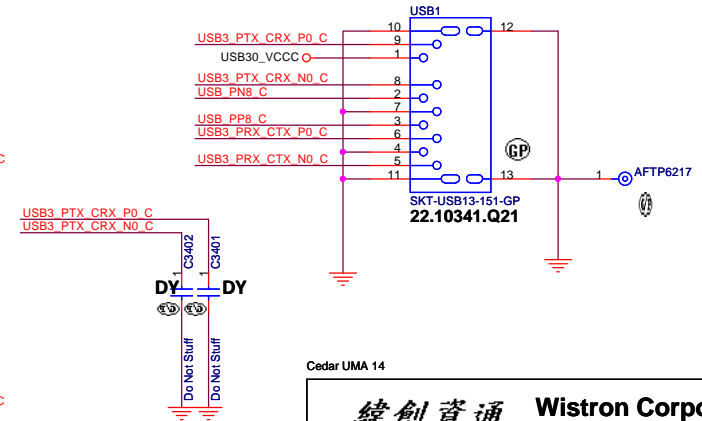
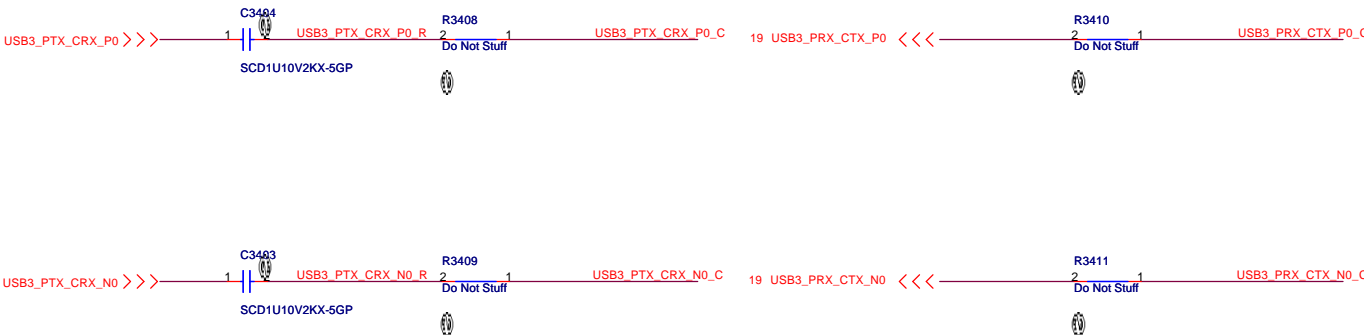
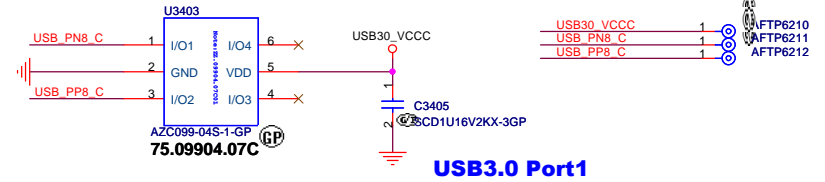
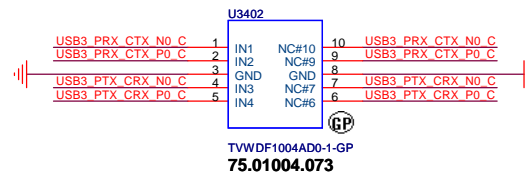
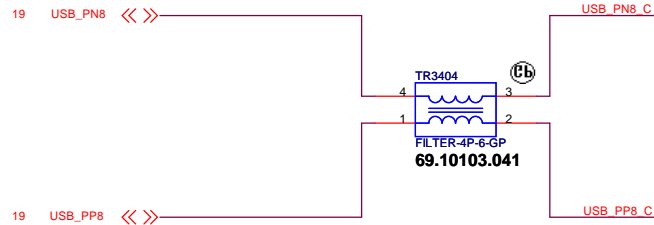
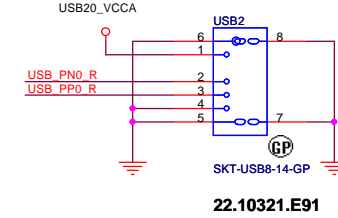
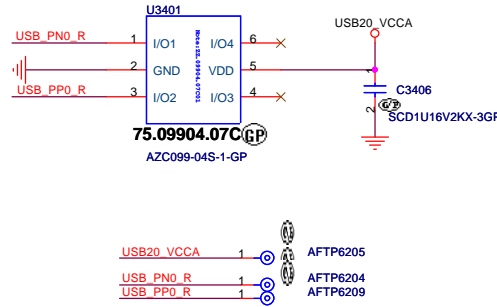
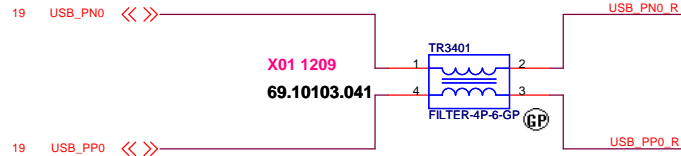
Cedar UMA 14

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
(Reserved)		
Size	Document Number	Rev
A4	Cedar AMD BEEMA	A00
Date: Wednesday, March 05, 2014		Sheet 33 of 104

SSID = USB

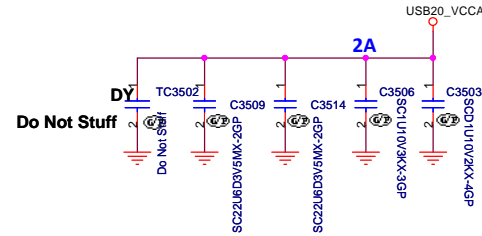
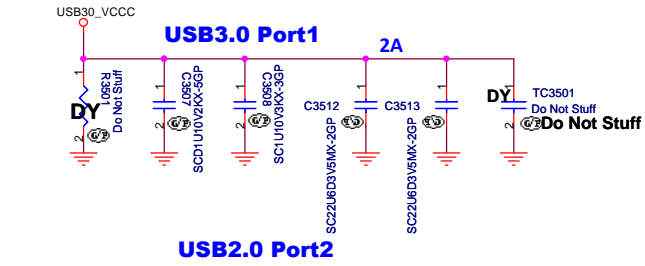
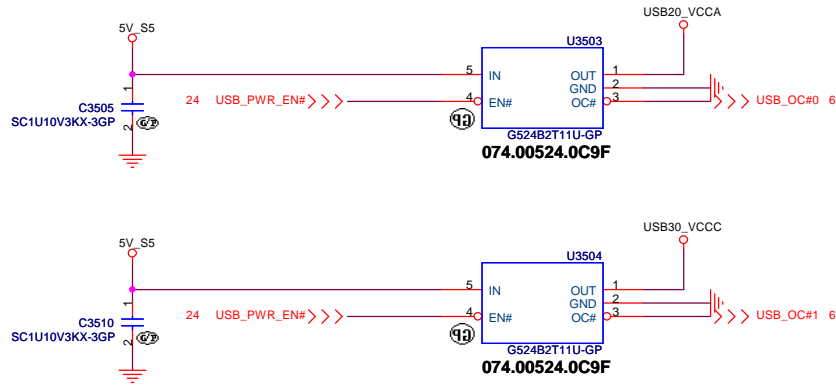
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USB2.0 Port2

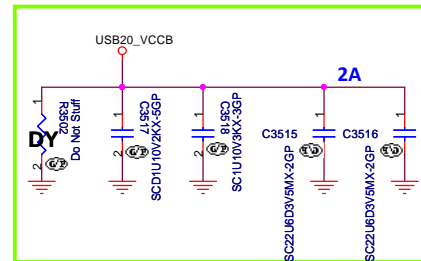
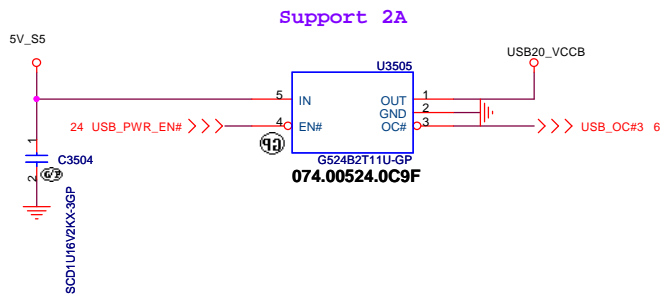


Cedar UMA 14

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Layout Note: Close CON1



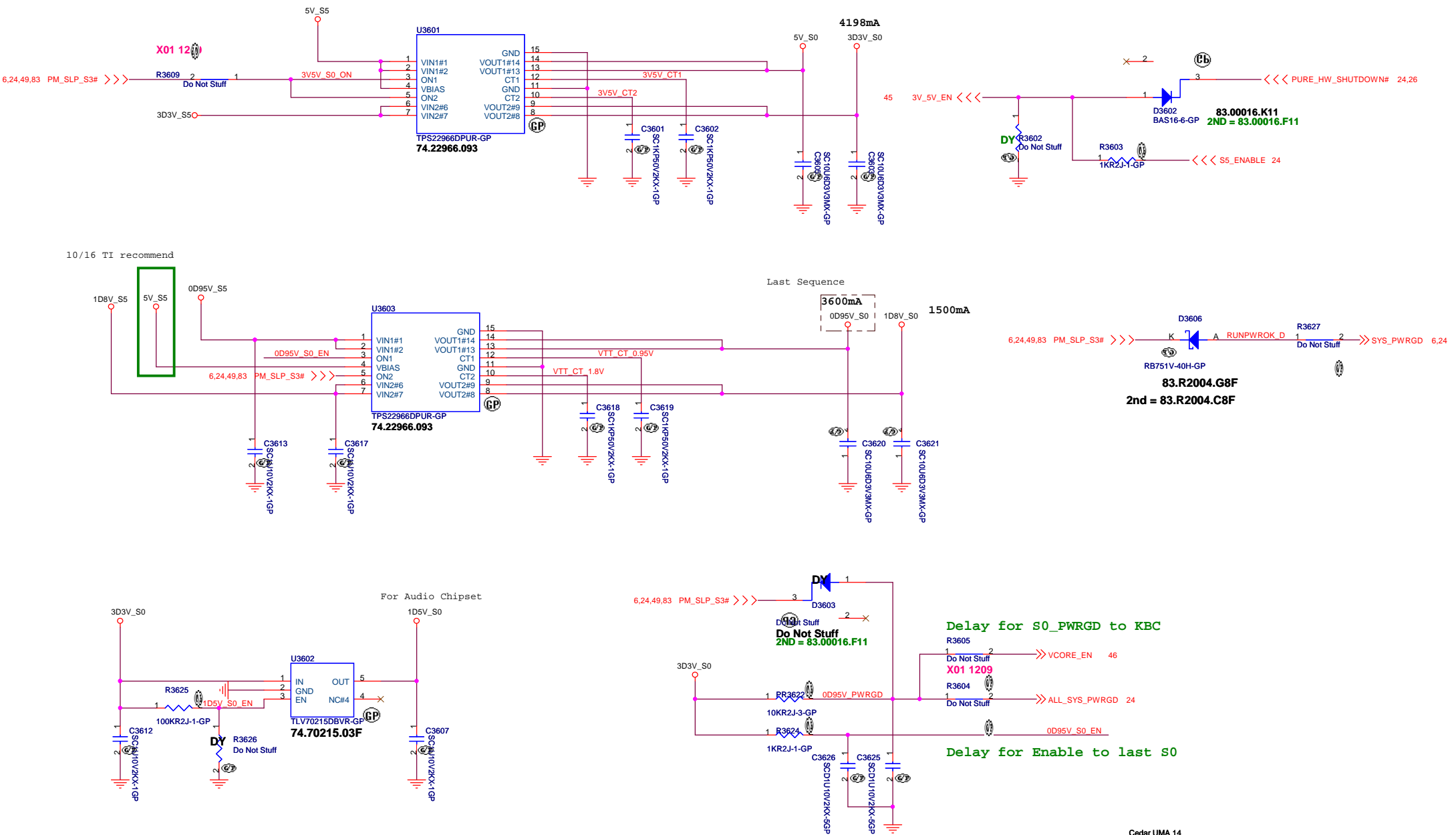
USB2.0 Port3 (IO Board)

Cedar UMA 14

緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title		
USB Power SW		
Size	Document Number	Rev
	Cedar AMD BEEMA	A00
Date:	Wednesday, March 05, 2014	Sheet 35 of 104

# Power Sequence



SSID = Reset.Suspend

(Blanking)

( Blanking )

Cedar UMA 14

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Title <div>(Reserved)</div>		
Size <div>A4</div>	Document Number <div>Cedar AMD BEEMA</div>	Rev <div>A00</div>
Date: Wednesday, March 05, 2014		Sheet 38 of 104

( Blanking )

Cedar UMA 14

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>(Reserved) 1D05_M</div>		
Size <div>A4</div>	Document Number <div>Cedar AMD BEEMA</div>	Rev <div>A00</div>
Date: Wednesday, March 05, 2014		Sheet 39 of 104

( Blanking )

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<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
Reserved		
Size A4	Document Number Cedar AMD BEEMA	Rev A00
Date: Wednesday, March 05, 2014		
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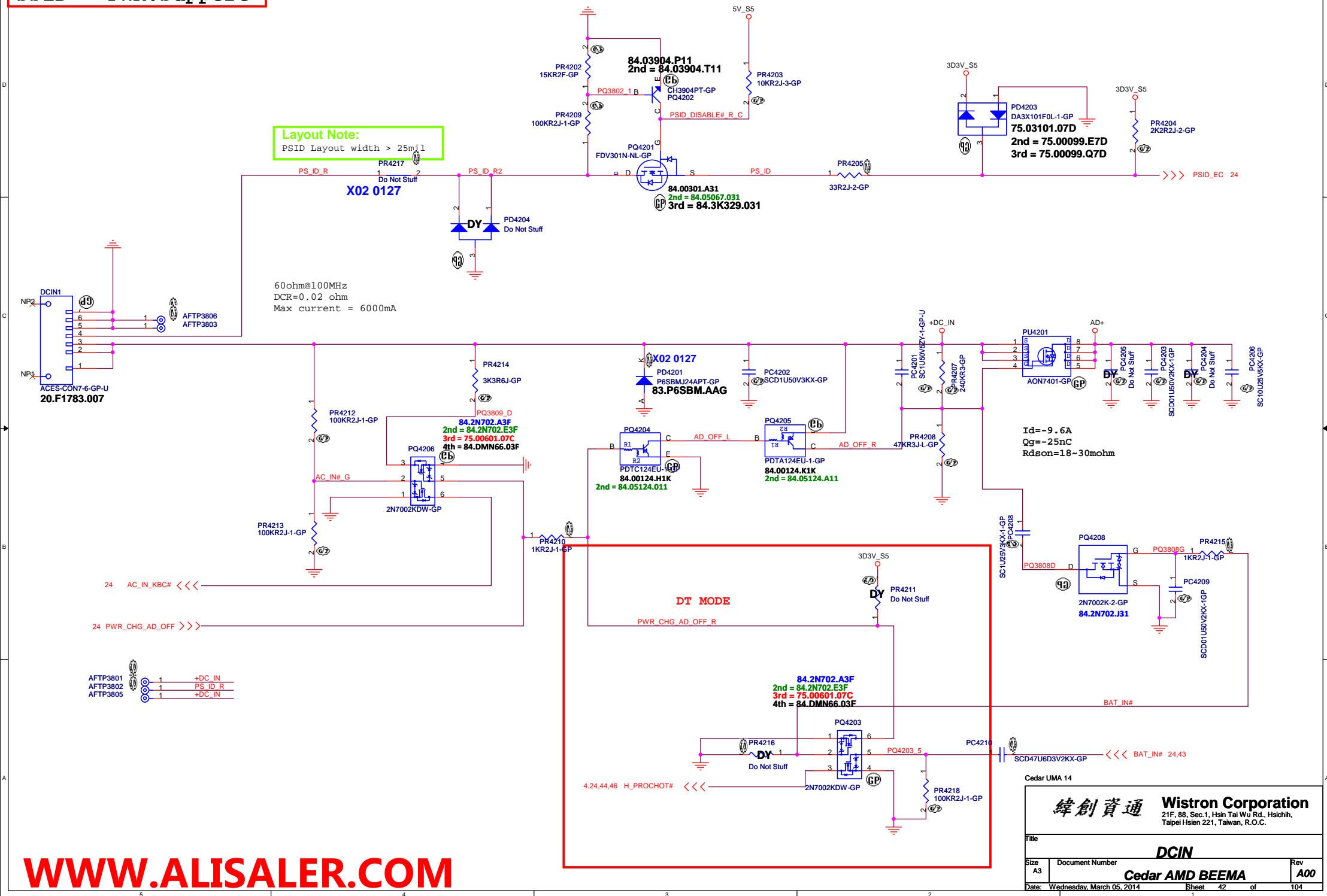


(Blanking)

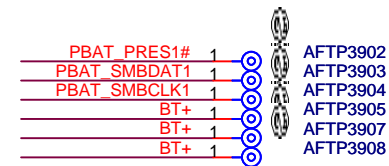
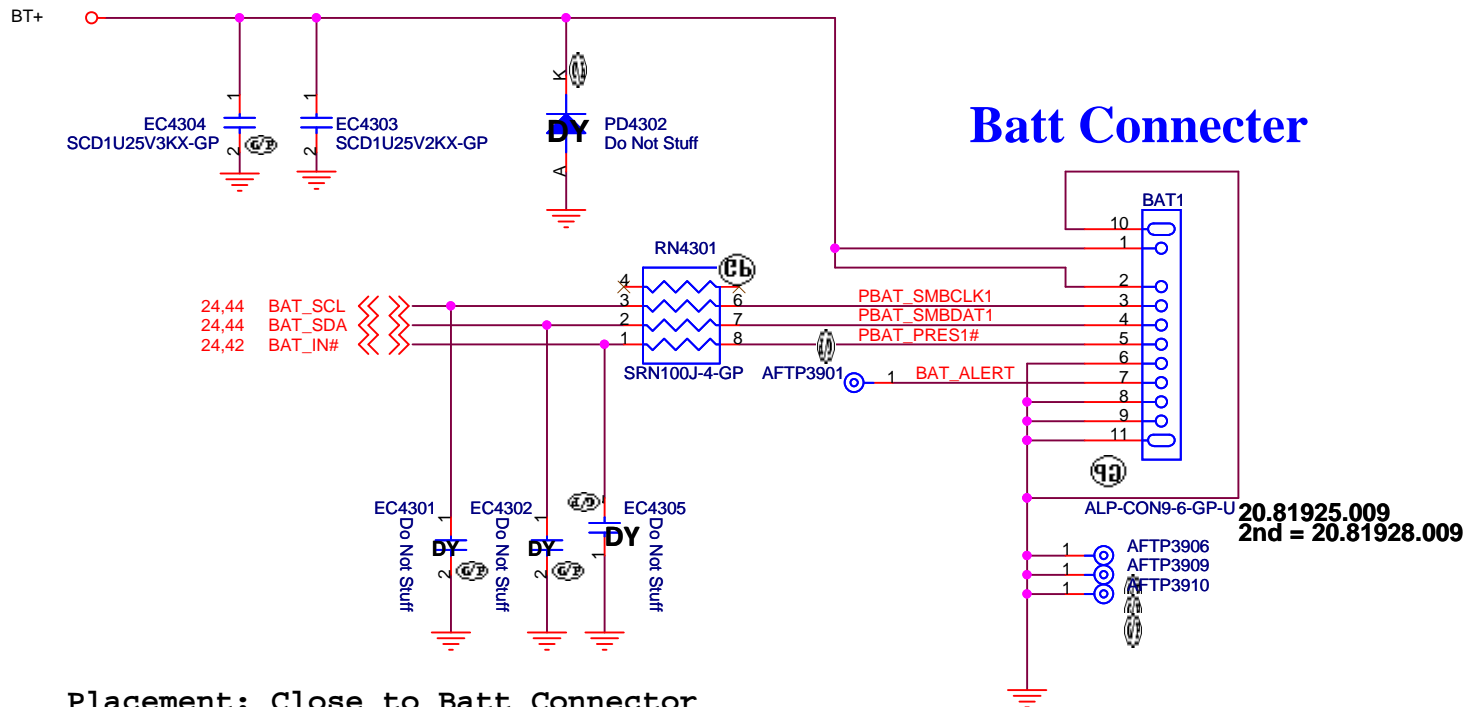
Cedar UMA 14

<div>緯創資通</div>		<div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
Title			
Reserved			
Size	Document Number		Rev
A4	Cedar AMD BEEMA		A00
Date:	Wednesday, March 05, 2014	Sheet 41 of	104

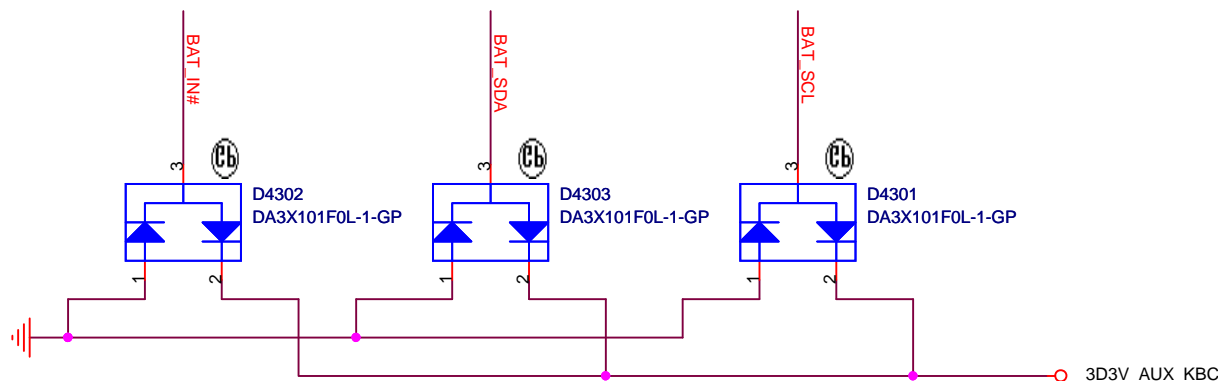
```
SSID = PWR.Support
```



SSID = PWR.Support



Placement: Close to Batt Connector



75.03101.07D

2nd = 75.00099.E7D

3rd = 75.00099.Q7D

75.03101.07D

2nd = 75.00099.E7D

3rd = 75.00099.Q7D

75.03101.07D

2nd = 75.00099.E7D

3rd = 75.00099.Q7D

Cedar UMA 14

緯創資通

Wistron Corporation

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Taipei Hsien 221, Taiwan, R.O.C.

Title

BATT CONN

Size  
A4

Document Number

Cedar AMD BEEMA

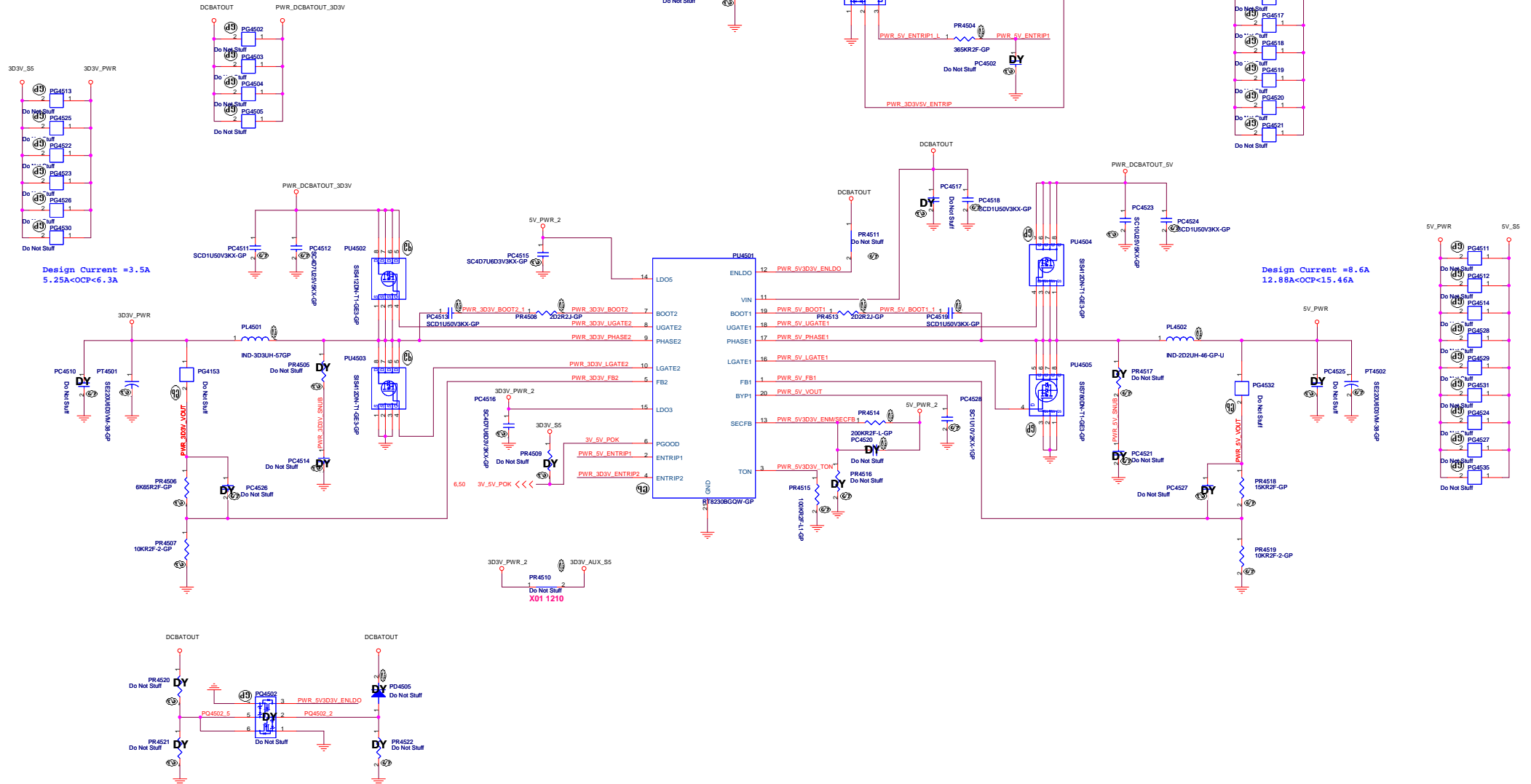
Rev  
A00

Date: Wednesday, March 05, 2014

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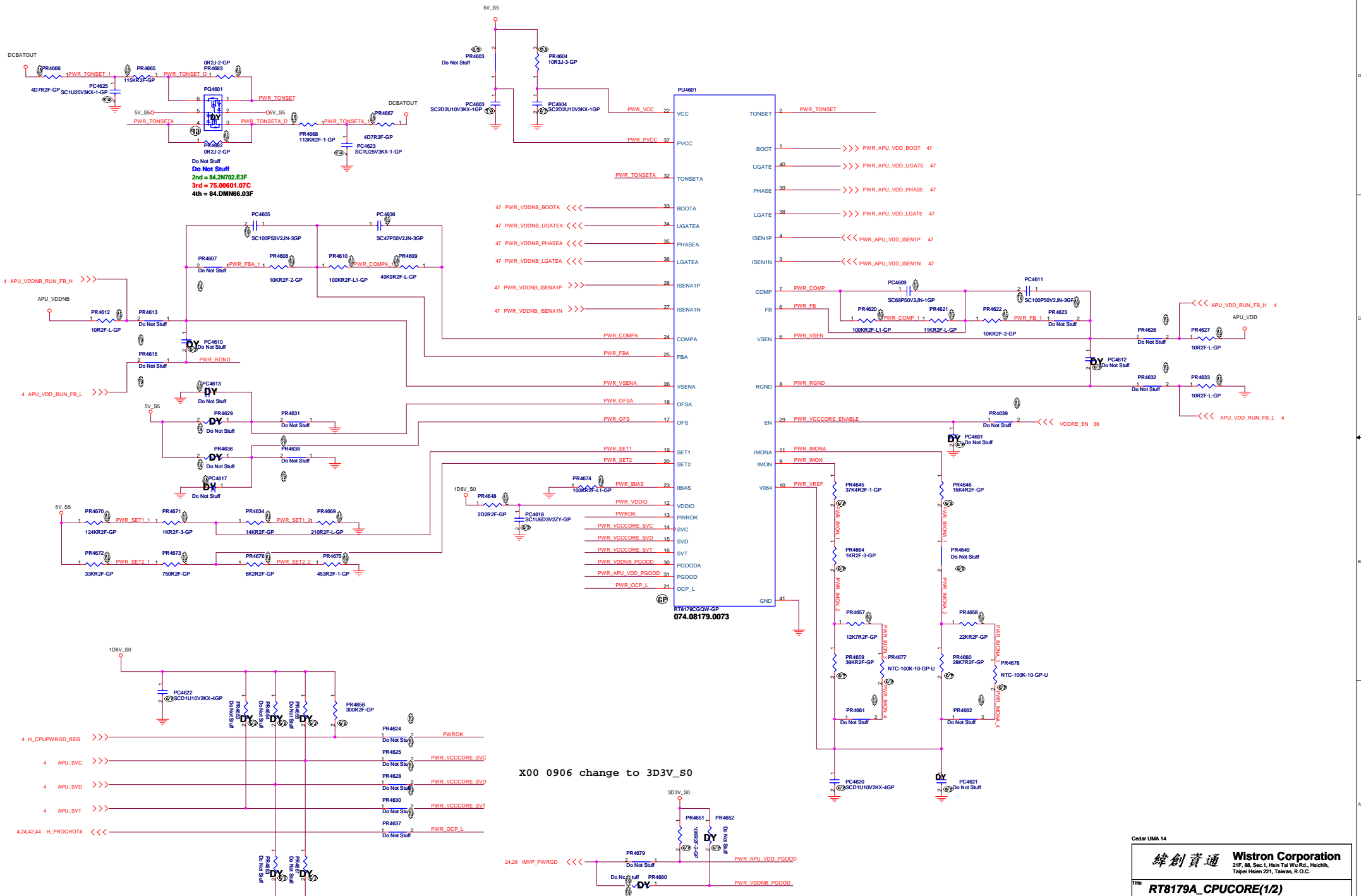


SSID = PWR.Plane.Regulator\_5v3p3v

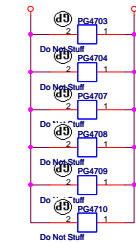


I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L  
Inductor: CHIP IND 3.3UH PCMC063T-3R3MN Cyntec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A  
O/P cap:CHIP CAP EL 220U 6.3V M6.3\*4.4 /Chemi-con/ 18mOhm / 79.22710.3KL  
H/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037  
L/S:SIS780 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L  
Inductor: CHIP CHOKE 2.2U PCMC063T-2R2MN 18mohm/20mohm Isat =14Arms 68.2R210.20B  
O/P cap:CHIP CAP EL 220U 6.3V M6.3\*4.4 /Chemi-con/ 18mOhm / 79.22710.3KL  
H/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037  
L/S:SIS780 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037



DCBATOUT PWR\_APU\_VDD\_DCBATOUT



46 PWR\_APU\_VDD\_UGATE >>>

46 PWR\_APU\_VDD\_LGATE >>>

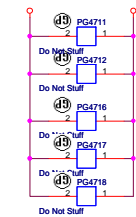
46 PWR\_APU\_VDD\_PHASE >>>

46 PWR\_APU\_VDD\_BOOT >>>

46 PWR\_APU\_VDD\_ISEN1P <<<

46 PWR\_APU\_VDD\_ISEN1N <<<

DCBATOUT PWR\_APU\_VDDNB\_DCBATOUT



46 PWR\_VDDNB\_UGATE >>>

46 PWR\_VDDNB\_LGATE >>>

46 PWR\_VDDNB\_PHASE >>>

46 PWR\_VDDNB\_BOOTA >>>

46 PWR\_VDDNB\_ISEN1P <<<

46 PWR\_VDDNB\_ISEN1N <<<

1st: 84.00920.037

1st: 84.00920.037

1st: 84.00920.037

1st: 84.00920.037

15W  
TDC=16A  
EDC=21A

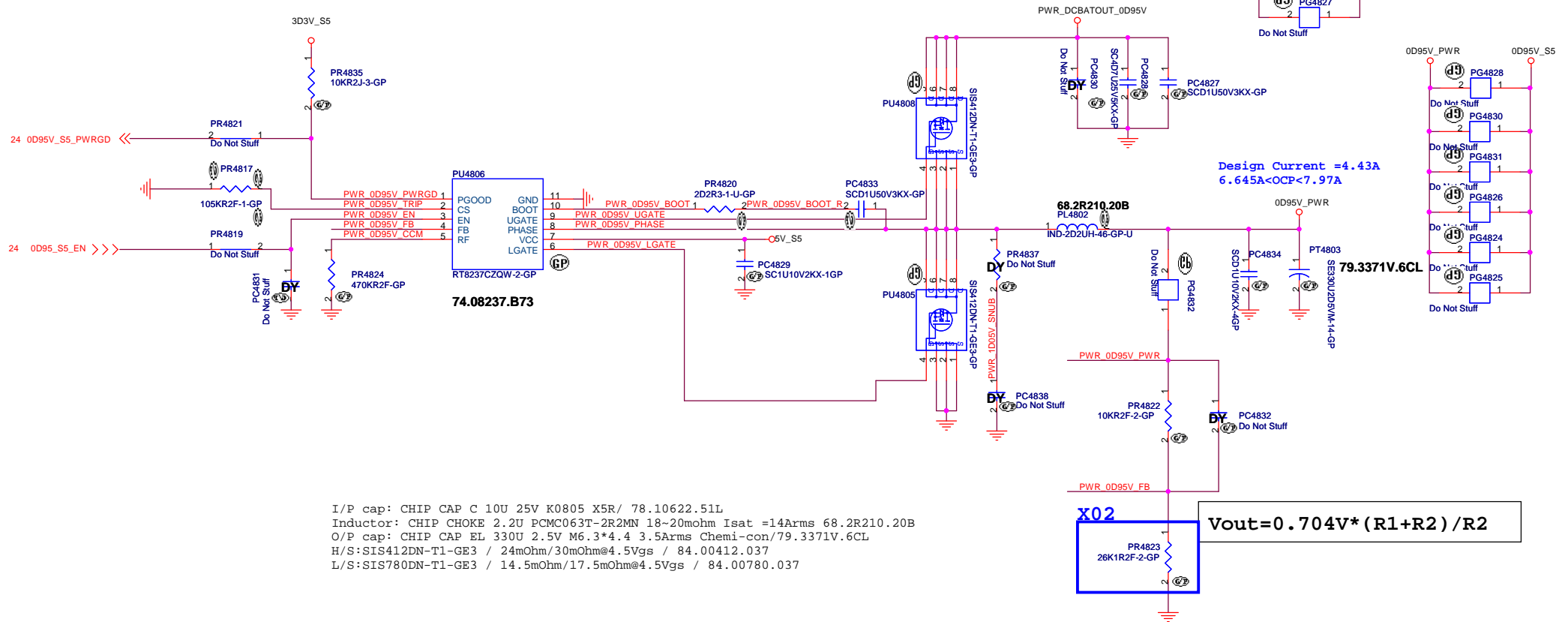
15W  
TDC=12A  
EDC=15A

Cedar UMA 14

緯創資通 Wistron Corporation	
21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
File	RT8179A_CPUCORE(22)
Size	Document Number
A2	Cedar AMD BEEMA
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Rev	A00

I/P cap: CHIP CAP C 10U 25V K0805 XSR/ 78.10622.51L  
Inductor: CHIP CHOK 0.36UH PCMR064T-R36MS1R407 1.4mohm / Isat =24Arms 68.R3610.20W  
O/P cap:CHIP CAP 470UF 2V EFPSX0D471X /Panasonic/ 6mOhm / 79.47719.2BL  
Dual N FET MOS SI2920DT-T1-GE3 DUAL NC POWER 8P /H/S 7.4mohm/8.9mohm / L/S 2.9mOhm/3.5mohm@4.5Vgs / 84.00920.037

SSID = PWR.Plane.Regulator\_1p05v



Cedar UMA 14

緯創資通

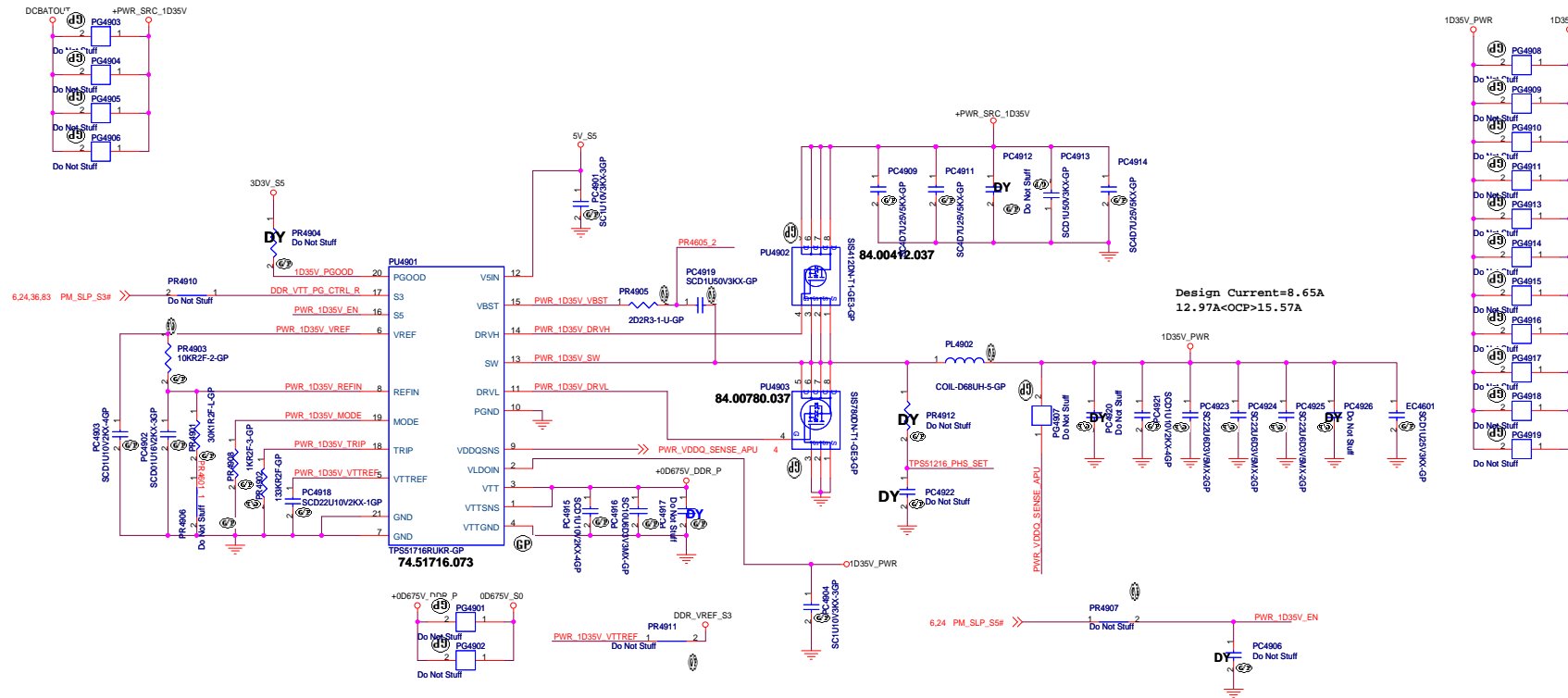
Wistron Corporation  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

Title  
**RT8237\_0D95V**

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```
SSID = PWR.Plane.Regulator 1p35v0p675v
```



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

```
I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 0.1UH M PCMC063T-R10NM 1.5-1.7mohm Isat =60Arms 68.R1010.10T
O/P cap: CHIP CAP C 22U 6.3V M0805 X5R /78.22610.51L
H/S:SI5412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SI5780 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037
```

TPS51716 MODE

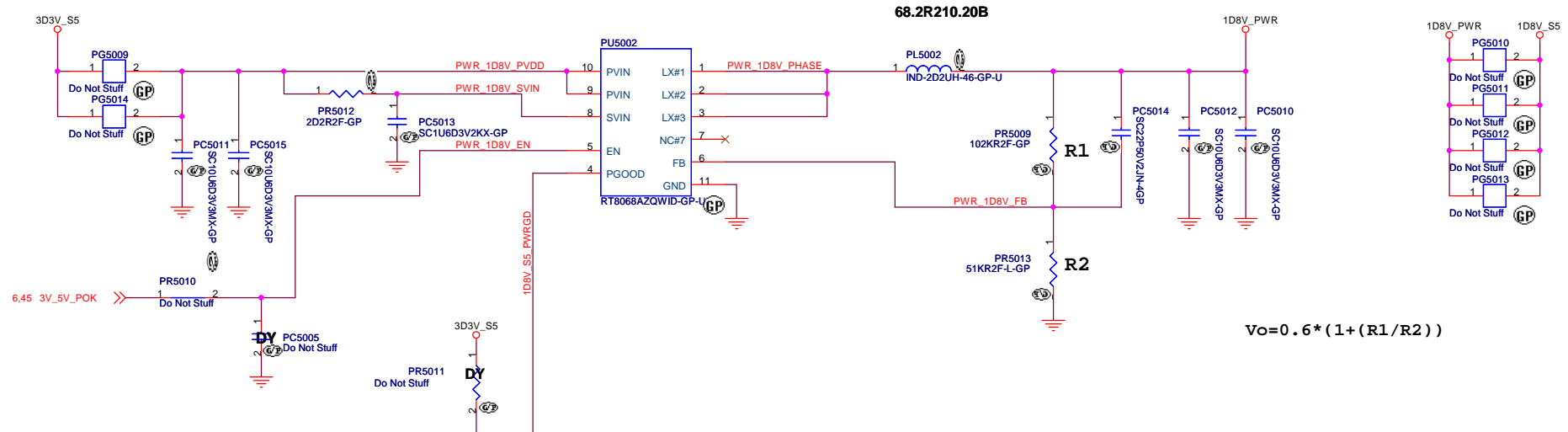
PR4608	Frequency	Discharge Mode
33k ohm	500kHz	Non-tracking Discharge
22k ohm	670kHz	
12k ohm	670kHz	Tracking Discharge
1k ohm	500kHz	

Cedar UMA 14

SSID = PWR.Plane.Regulator\_1p8v

# RT8068A for 1D8V\_S5

Design Current=1.62A



Cedar UMA 14

緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title			RT8068A 1D8V_S5	
Size	Document Number		Rev	
A3	Cedar AMD BEEMA		A00	
Date:	Wednesday, March 05, 2014		Sheet	50 of 104

SSID = PWR.Plane.Regulator\_1p5v

(Blanking)

Cedar UMA 14

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

TLV70215\_1D5

Size

A3

Document Number

Cedar AMD BEEMA

Rev

A00

Date:

Wednesday, March 05, 2014

Sheet

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104



EE note: Never change R5232 to short pad after MP  
Reserved for one time fuse: 69.43001.201

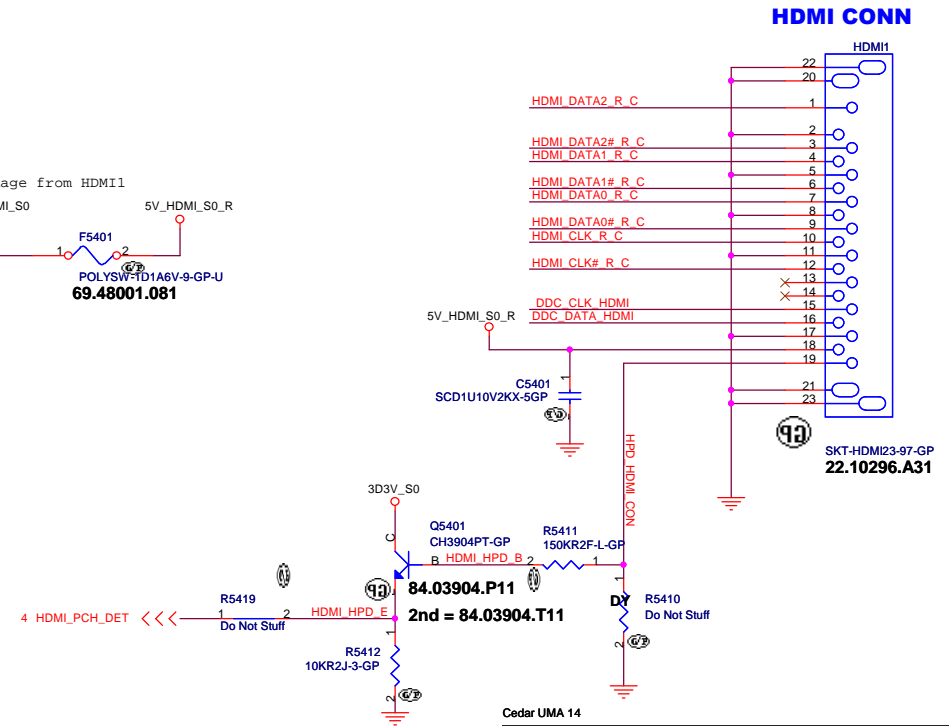
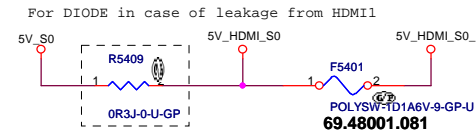
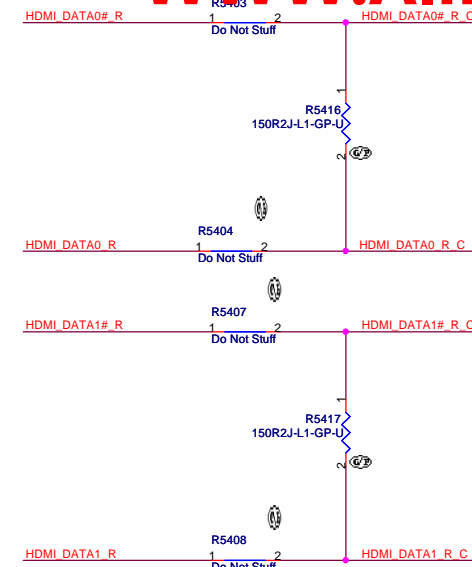
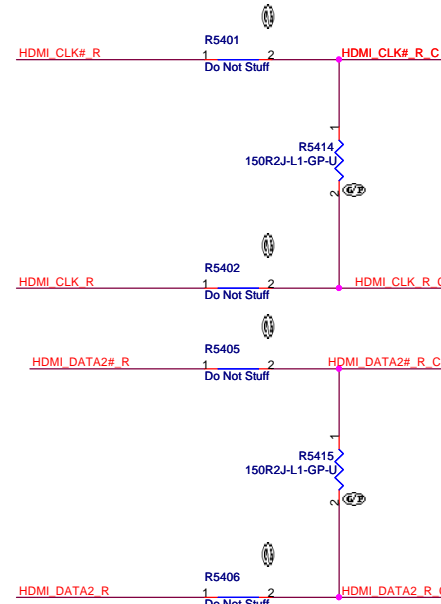
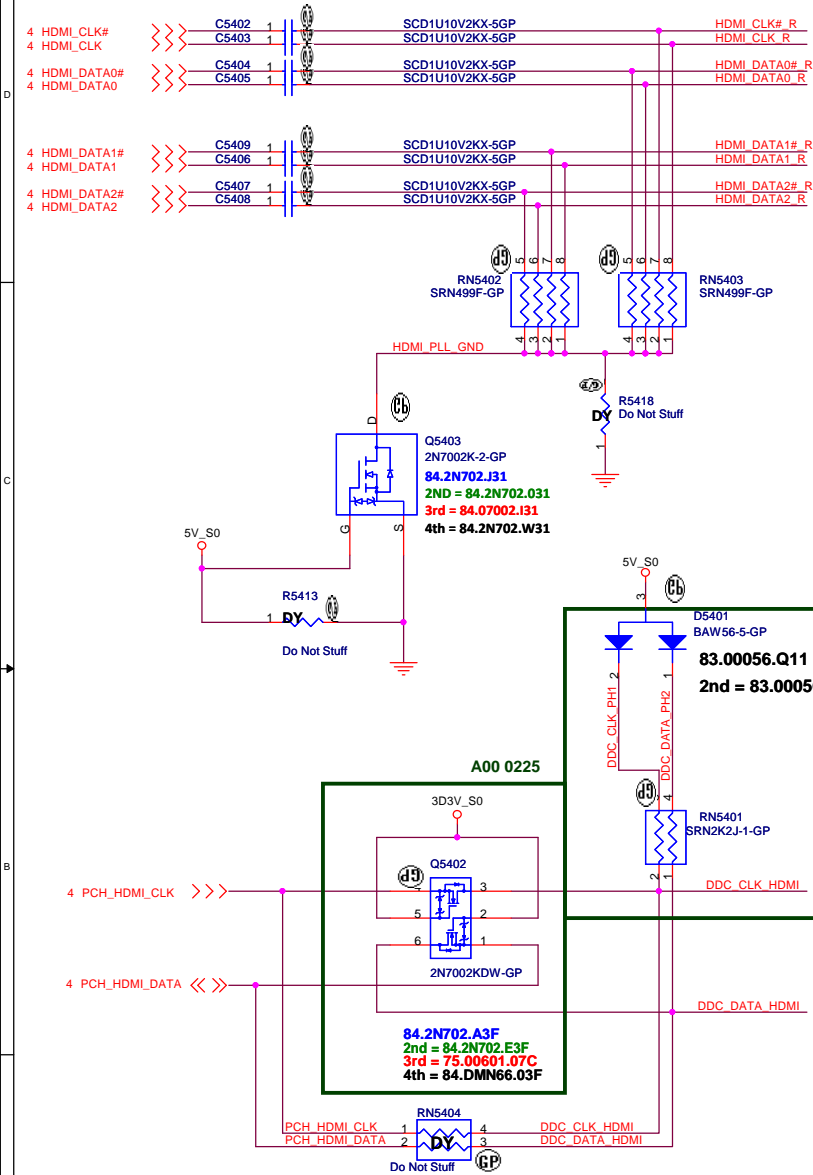
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Cedar UMA 14

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
(Reserved)			
Size	Document Number		Rev
A3	Cedar AMD BEEMA		A00
Date: Wednesday, March 05, 2014		Sheet 53 of 104	

SSID = VIDEO

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緯創資通 Wistron Corporation  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

Title		
HDMI Level Shifter/Connector		
Size	Document Number	Rev
A3		A00
Date:	Wednesday, March 05, 2014	Sheet 54 of 104

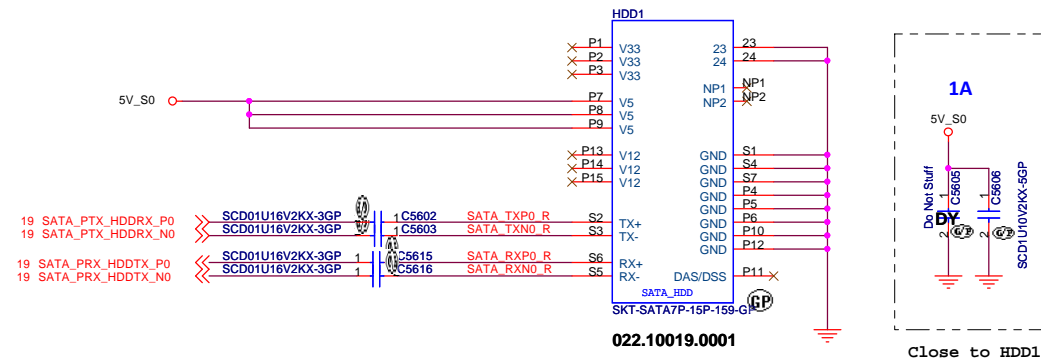
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(Blanking)

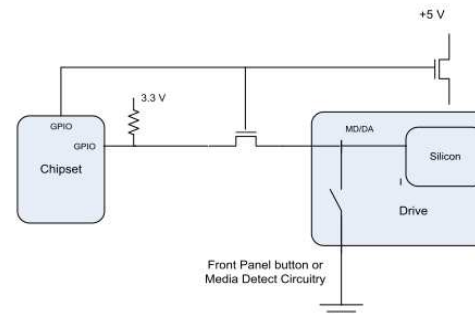
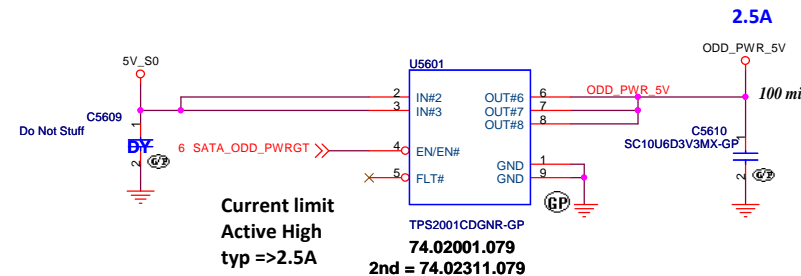
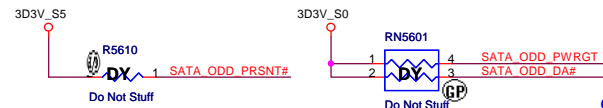
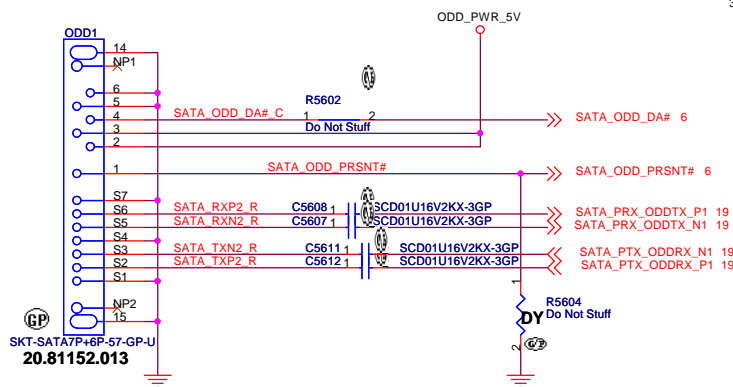
Cedar UMA 14

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
VGA Con.(Reserve)			
Size	Document Number	Rev	
A3	Cedar AMD BEEMA	A00	
Date: Wednesday, March 06, 2014		Sheet	55 of 104

## SATA HDD Connector



## ODD Connector



Cedar UMA 14

**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **HDD/ODD**

Size A3 Document Number: **Cedar AMD BEEMA** Rev: **A00**

Date: Wednesday, March 05, 2014 Sheet 56 of 104

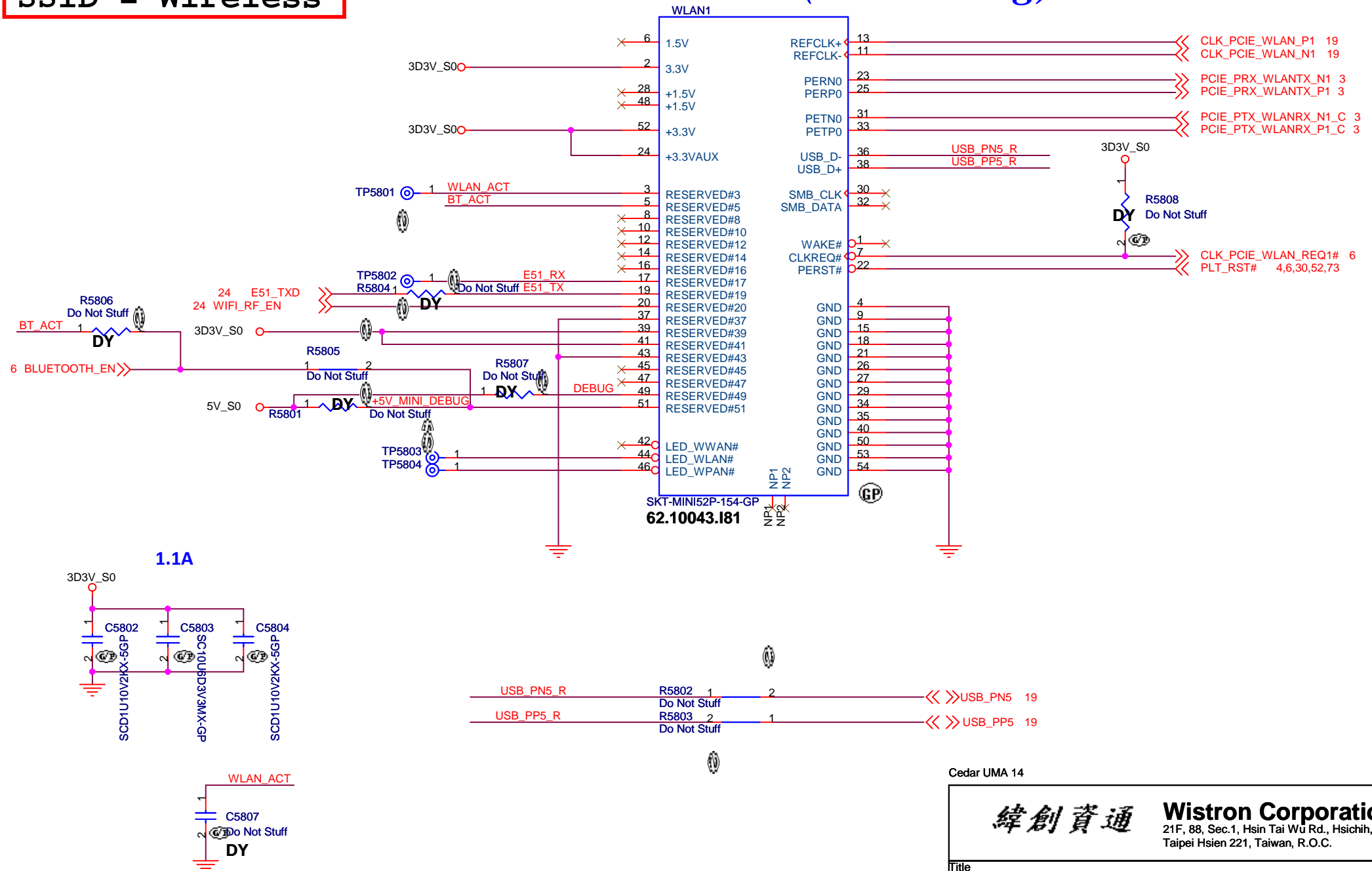


SSID = ESATA

( Blanking )

## SSID = Wireless

## Mini Card Connector(802.11a/b/g)



(Blanking)

Cedar UMA 14

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>Cedar AMD BEEMA</div>	Rev <div>A00</div>
Date: Wednesday, March 05, 2014		Sheet 59 of 104

( Blanking )

Cedar UMA 14

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>(Reserved)</div>		
Size <div>A4</div>	Document Number <div>Cedar AMD BEEMA</div>	Rev <div>A00</div>
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24 KBC\_PWRBTN# <<

R6102

100R2J-2-GP

AFTP6801

EC6104

Do Not Stuff

SW1

ETX-CON4-34-GP

20.K0465.004

20.K0382.004

AFTP6802

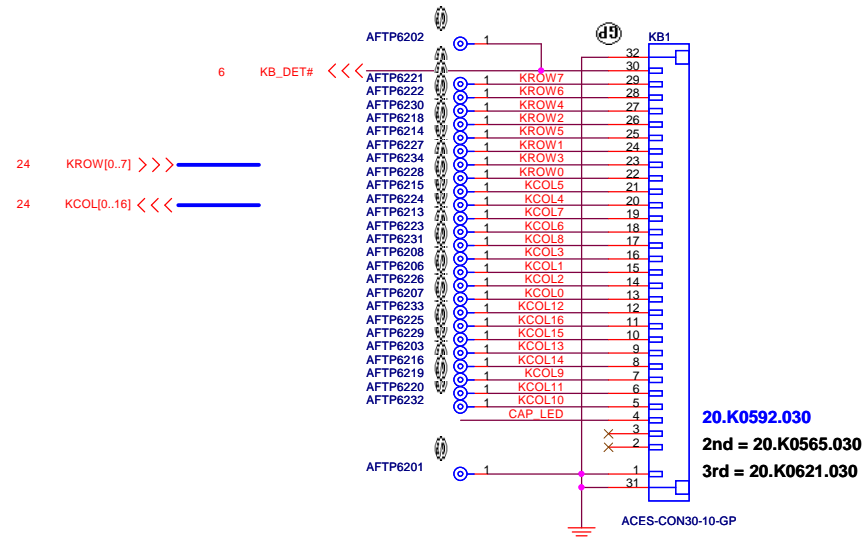
**SSID = KBC**

```
SSID = Touch.Pad
```

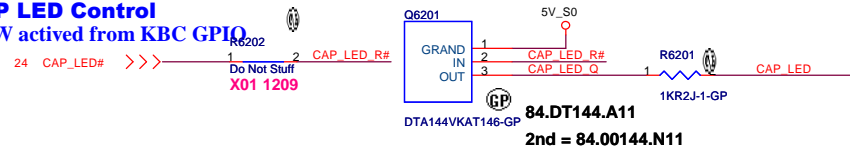
2 1

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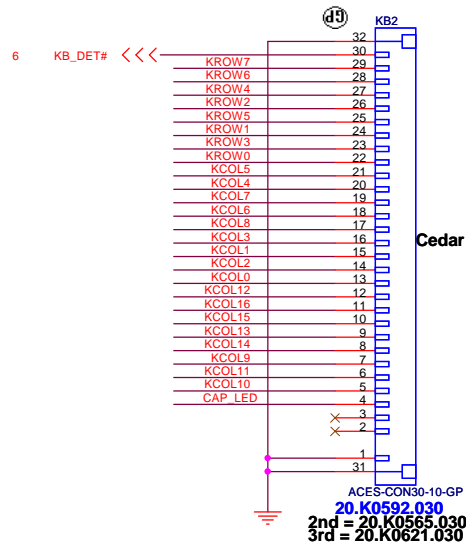
## Internal Keyboard Connector (DVC40)



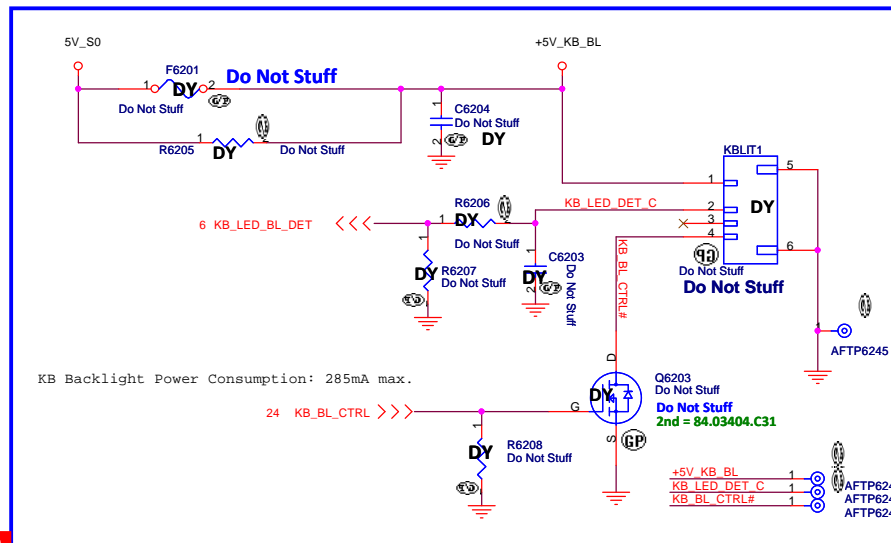
**CAP LED Control**  
LOW actived from KBC GPIO



## Internal Keyboard Connector (DVC50)

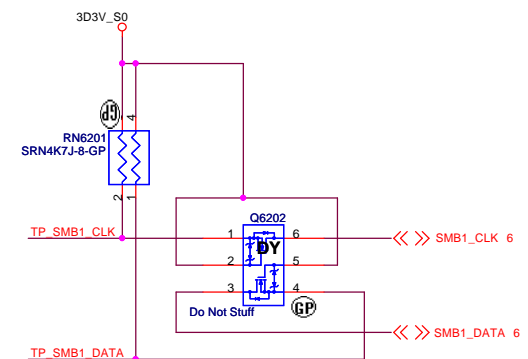
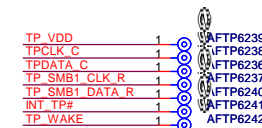
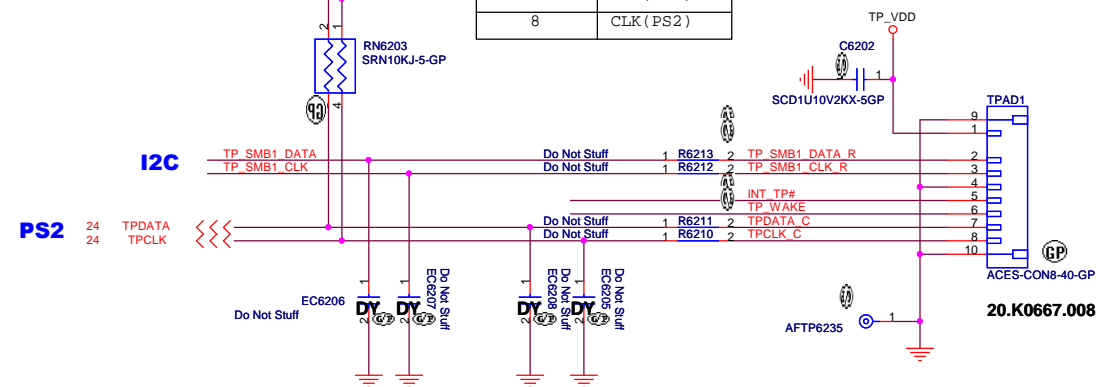


## Keyboard Backlight



Pin number	Pin name
1	VDD
2	DAT(I2C)
3	CLK(I2C)
4	GND
5	ATTN
6	GPIO
7	DAT(PS2)
8	CLK(PS2)

## Touch Pad Connector



Cedar UMA 14

緯創資通

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

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### **Key Board/Touch Pad**

Size

e	Document Number
---	-----------------

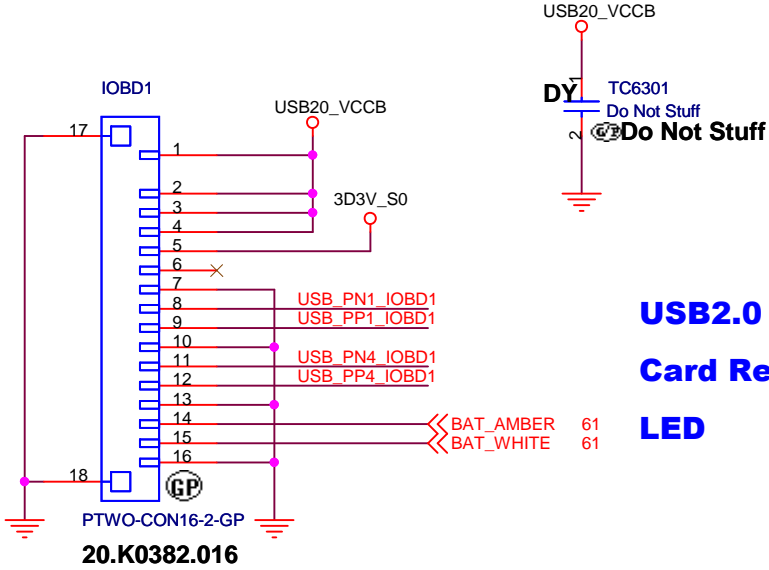
Number \_\_\_\_\_

Rev	1.00
-----	------

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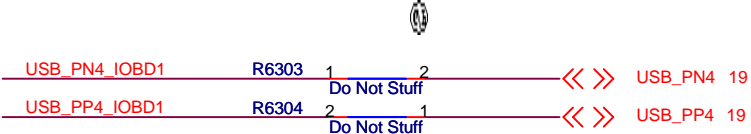
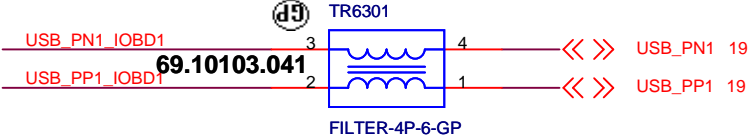
**WWW.ALISALER.COM**



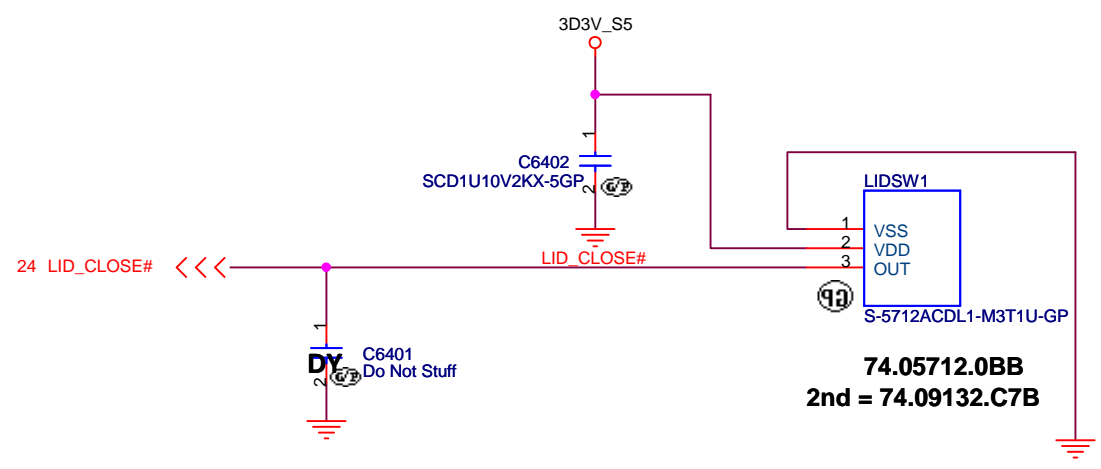
**USB2.0 Port3**

**Card Reader**

**LED**



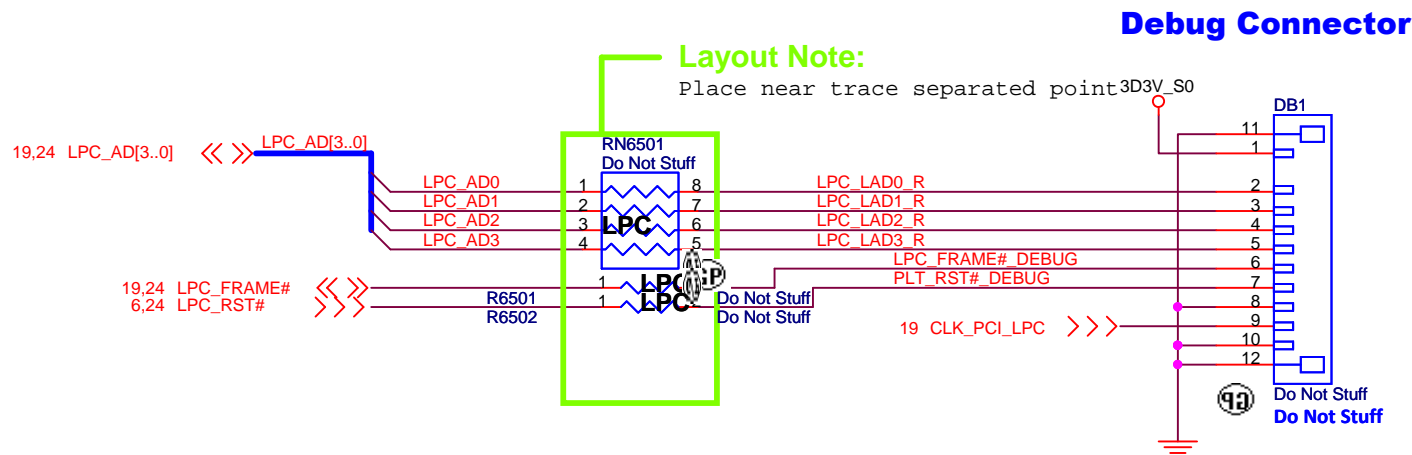
The maximum range of the PMOS output current in RTS5170 (Card Reader IC) is 400mA



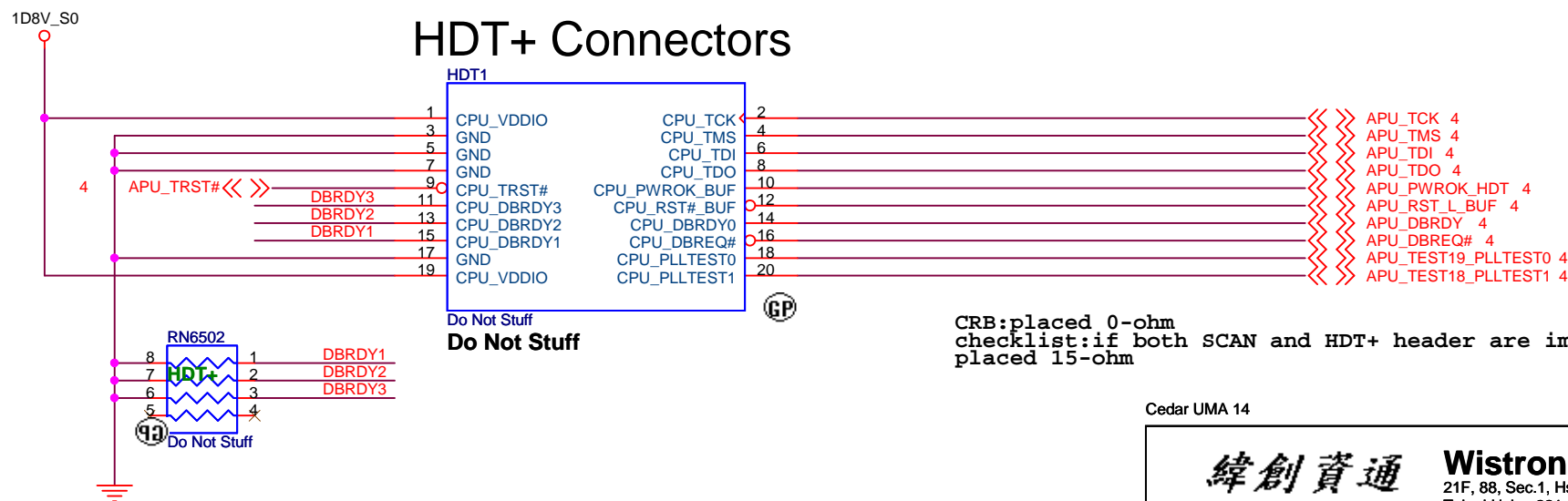
Cedar UMA 14

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Title		
Hall Sensor		
Size A4	Document Number Cedar AMD BEEMA	Rev A00
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20.D0075.110: Dummy Pad with solder mask is ZZ.00PAD.Y41  
DB1 Optional: New one smaller LPC connector is 20.F1180.010.



Cedar UMA 14

緯創資通

**Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

Title

**Dubug connector**

Size  
A4

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**A00**

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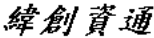
( Blanking )

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<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Reserved</b>			
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Title			
Reserved			
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Title <div>Thunderbolt (1/5)</div>		
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Title <div>Thunderbolt (2/5)</div>		
Size <div>A4</div>	Document Number <div>Cedar AMD BEEMA</div>	Rev <div>A00</div>
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Title <div>Thunderbolt (3/5)</div>		
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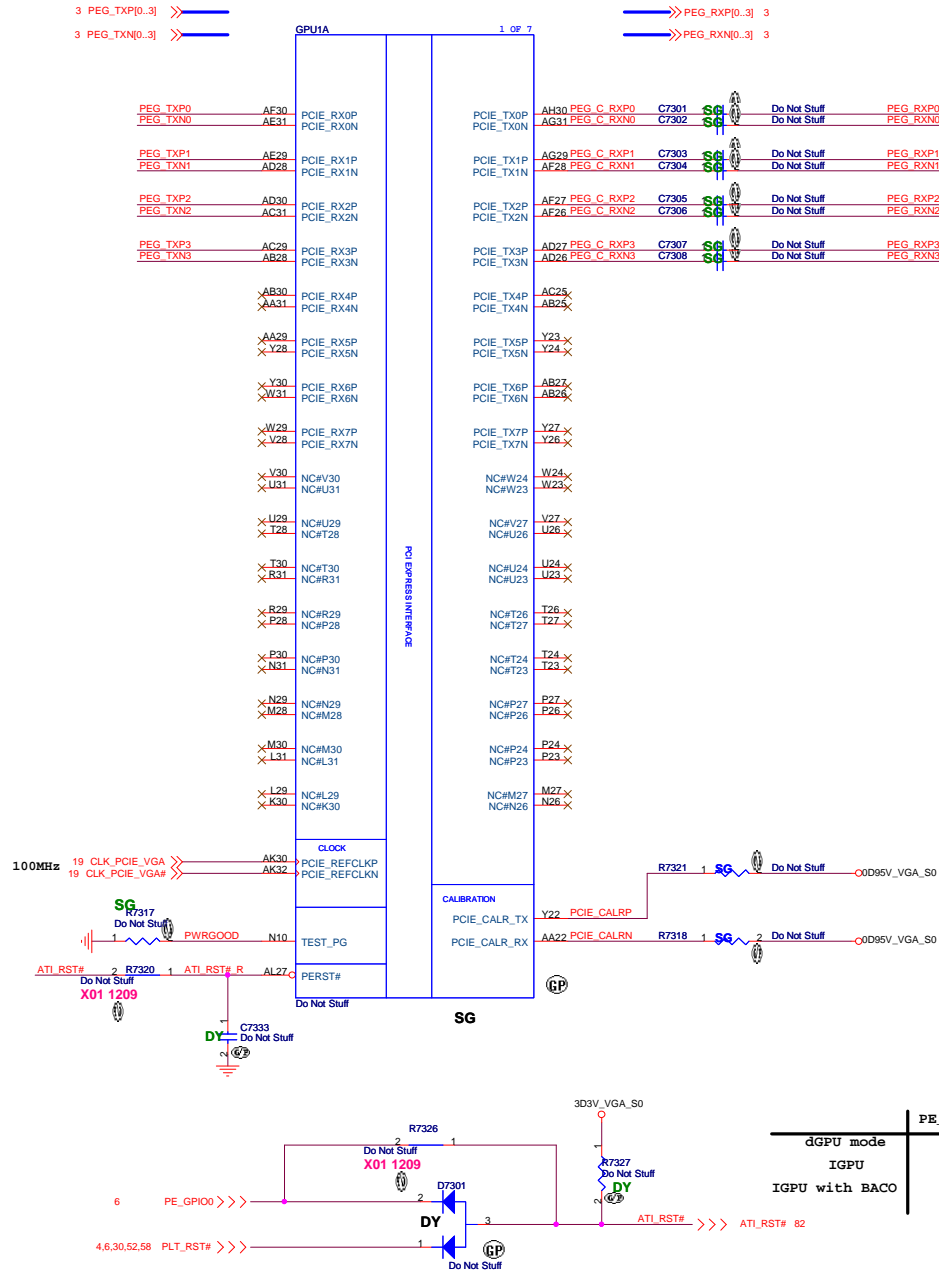
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Title <div>Thunderbolt (4/5)</div>		
Size <div>A4</div>	Document Number <div>Cedar AMD BEEMA</div>	Rev <div>A00</div>
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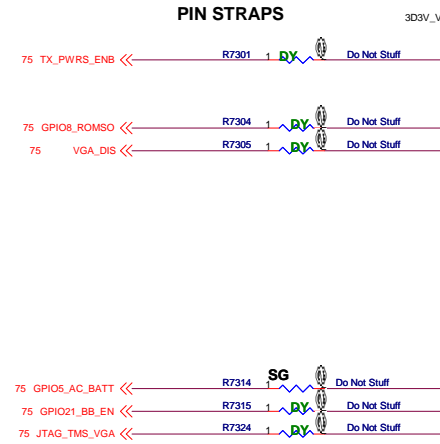
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<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Thunderbolt (5/5)</div>		
Size <div>A4</div>	Document Number <div>Cedar AMD BEEMA</div>	Rev <div>A00</div>
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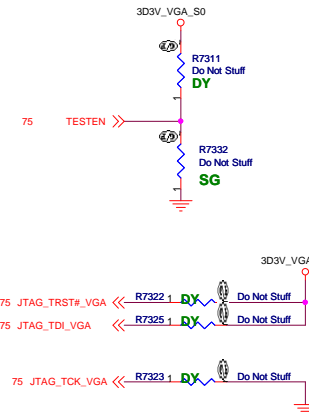


CONFIGURATION STRAPS			RECOMMENDED SETTINGS	
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET			0= DO NOT INSTALL RESISTOR 1= INSTALL 3K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE	
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMEND	PLATFORM SETTING
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X	1
TX_DEEMPH_EN	GPIO1	PCIe TRANSMITTER DE-EMPHASIS ENABLED 0:Tx de-emphasis disabled 1:Tx de-emphasis enabled	X	1
BIF_GEN2_EN_A	GPIO2	0:Advertises the PCIe device as 2.5GT/s capable at power on. 1:Advertises the PCIe device as 5.0GT/s capable at power on.	0	0
GPIO5_AC_BATT	GPIO5	optional input allow the system to request a fast power reduction by setting GPIO5 to low.	?	0
RESERVED	GPIO8	RESERVED	0	0
VGA_DIS	GPIO9	0:VGA Controller capacity enabled 1:The device won't be recognized as the system's VGA controller	0	0
ROMIDCFG[2:0]	GPIO[13:11]	BIOS_ROM_EN=1, Config[2:0] defines the ROM type BIOS_ROM_EN=0, Config[2:0] defines the primary memory aperture size	X X X	0 0 1 ( 256MB )
RESERVED	GPIO21	RESERVED	0	0
BIOS_ROM_EN	GPIO_22_ROMCSB	0:Disable external BIOS ROM device 1:Enable external BIOS ROM device	X	0
VIP_DEVICE_STRAP_EN	V2SYNC	VIP Device Strap Enable indicates to the software driver that it sense whether or not a VIP device is connected on the VIP Host interface.	X	0
RSVD	H2SYNC	RESERVED	0	0
RSVD	GENERICC	RESERVED	0	0
AUD[1]	HSYNC	AUD[1:0]:11-Audio for both DisplayPort and HDMI	X	1
AUD[0]	VSXNC		X	1



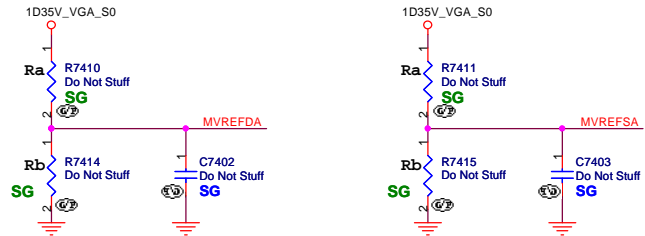
#### JTAG SIGNAL OPTION

Signal	Normal mode	Debug mode	pilot run mode
TESTEN	"1" (PU)	"1" (PU)	"0" (PD)
JTAG_TRST#	"0" (PD)	"1" (PU)	NC
JTAG_TCK	CLK	"1" (PU)	NC
JTAG_TMS	"1" (PU)	"1" (PU)	NC



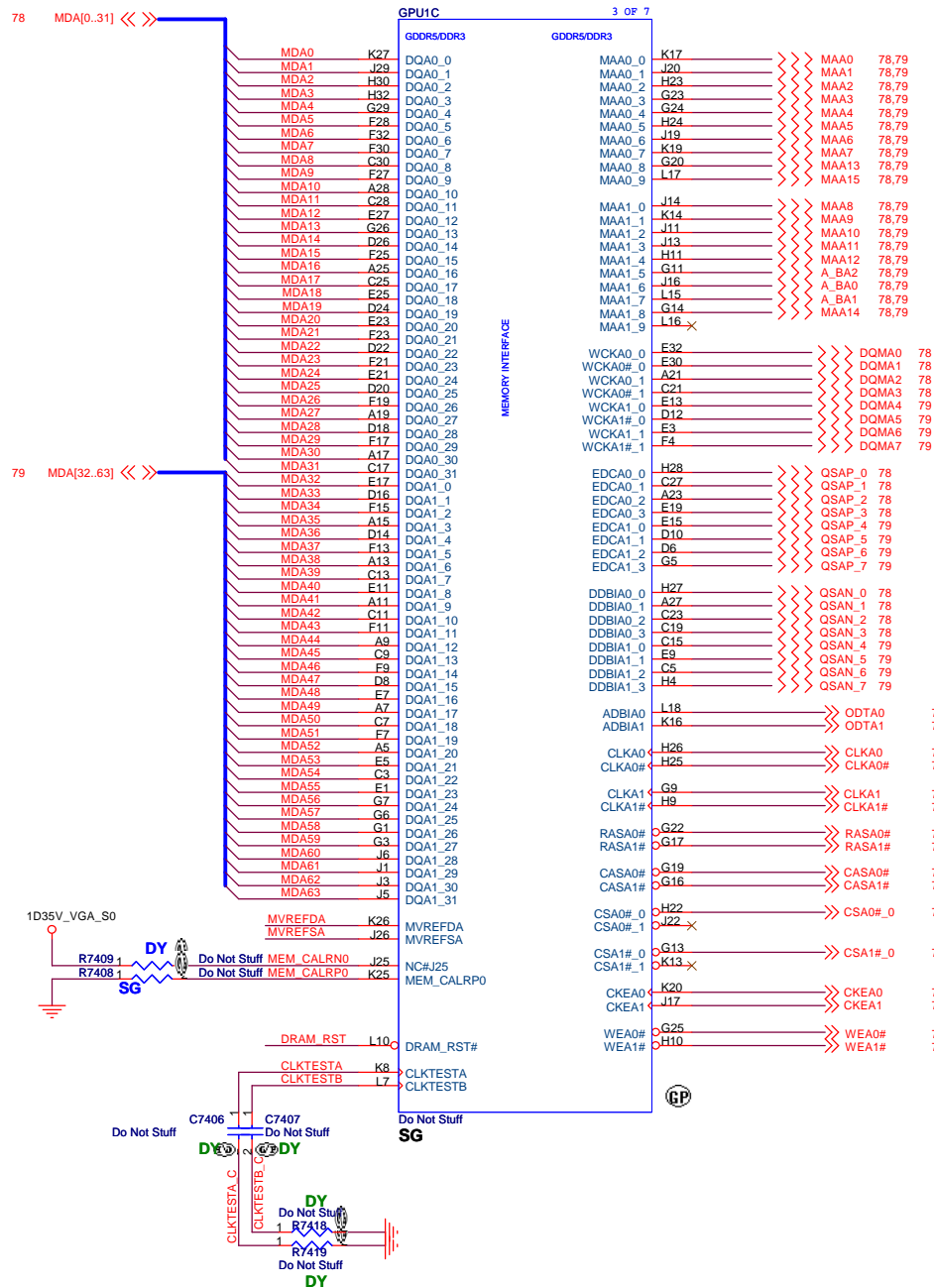
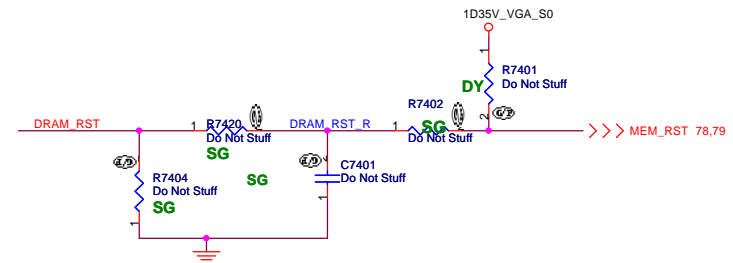
Cedar UMA 14

PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC



DDR3/GDDR3 Memory Stuff Option(Mad/Park)

	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1.8V/1.5V	1.35V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

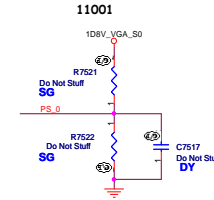
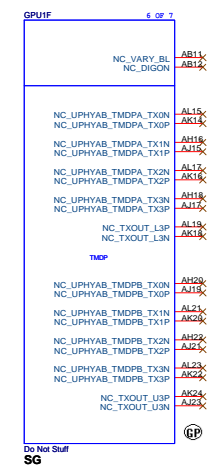
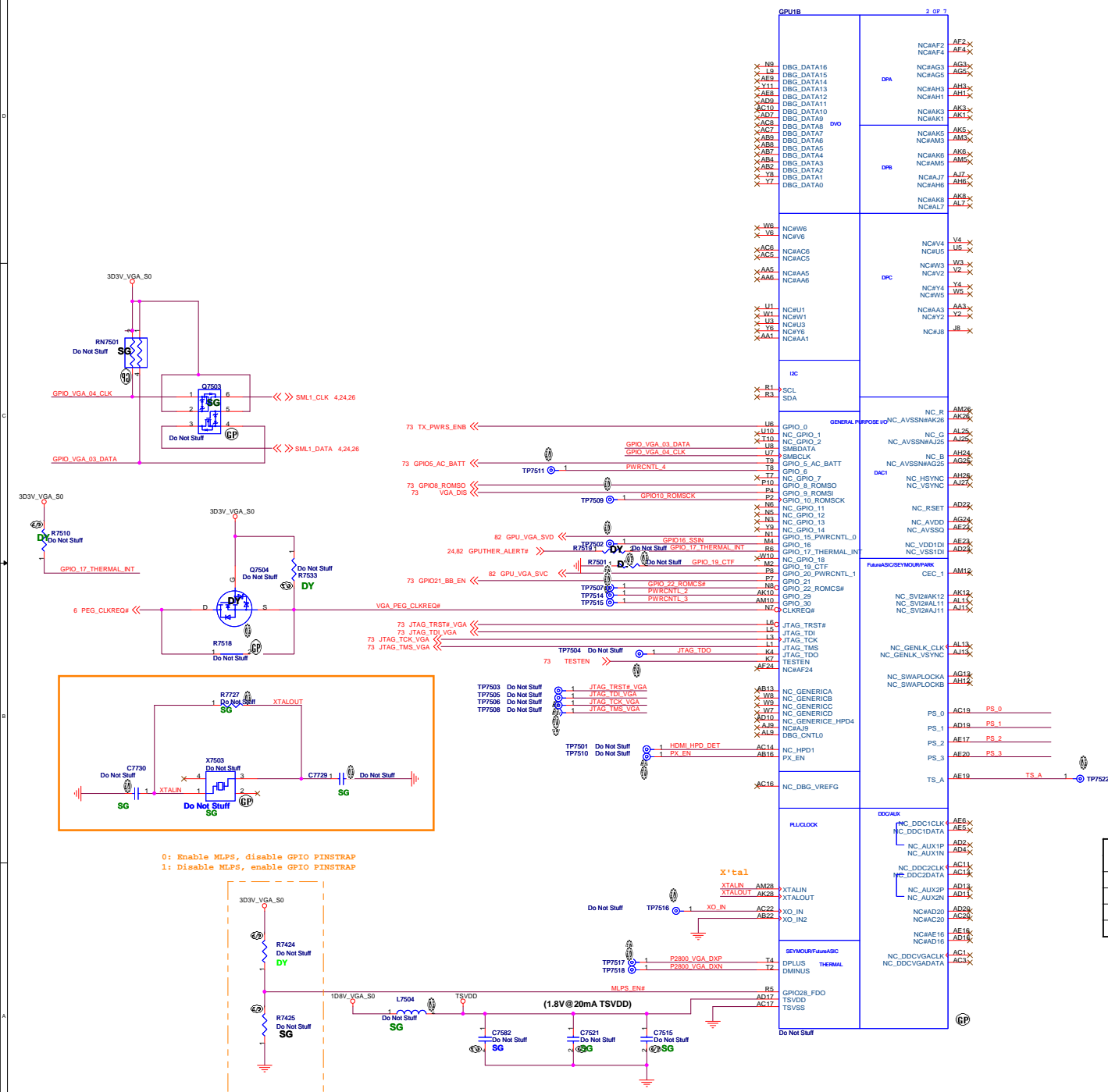


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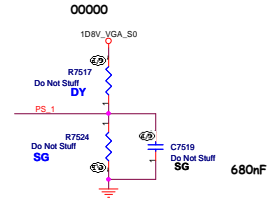
緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
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Title GPU\_Digitalout

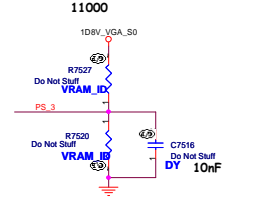
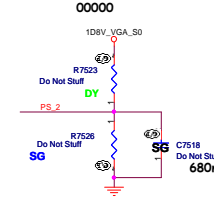
Size A3 Document Number Cedar AMD BEEMA Rev A00  
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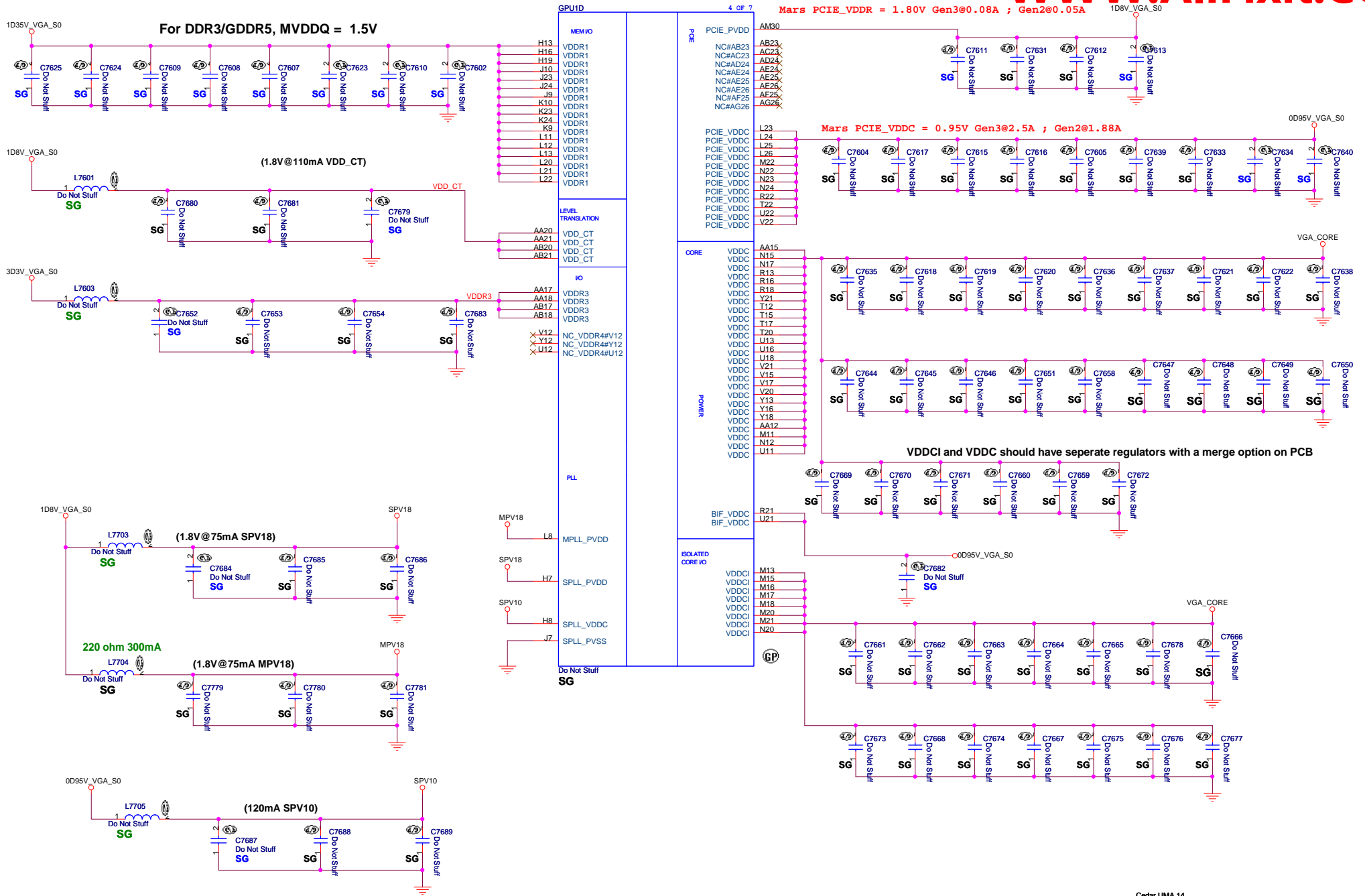
PS\_1[1]=1 => PCIe GEN3 is supported

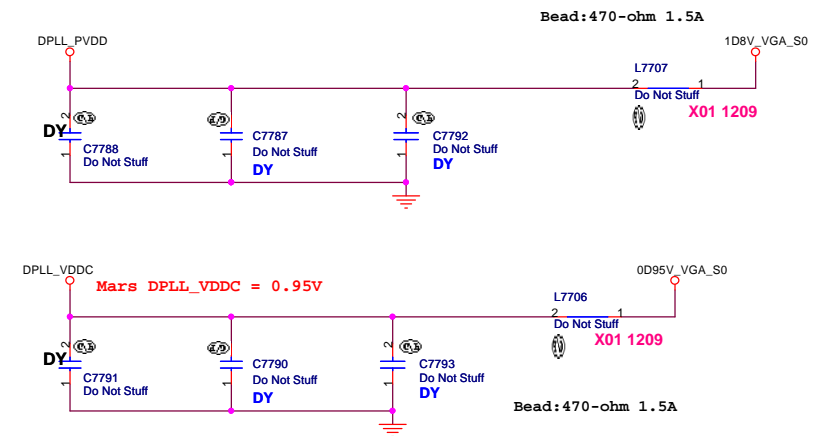


PS\_3[3-1] => MEM\_ID setting, need decide for AMD

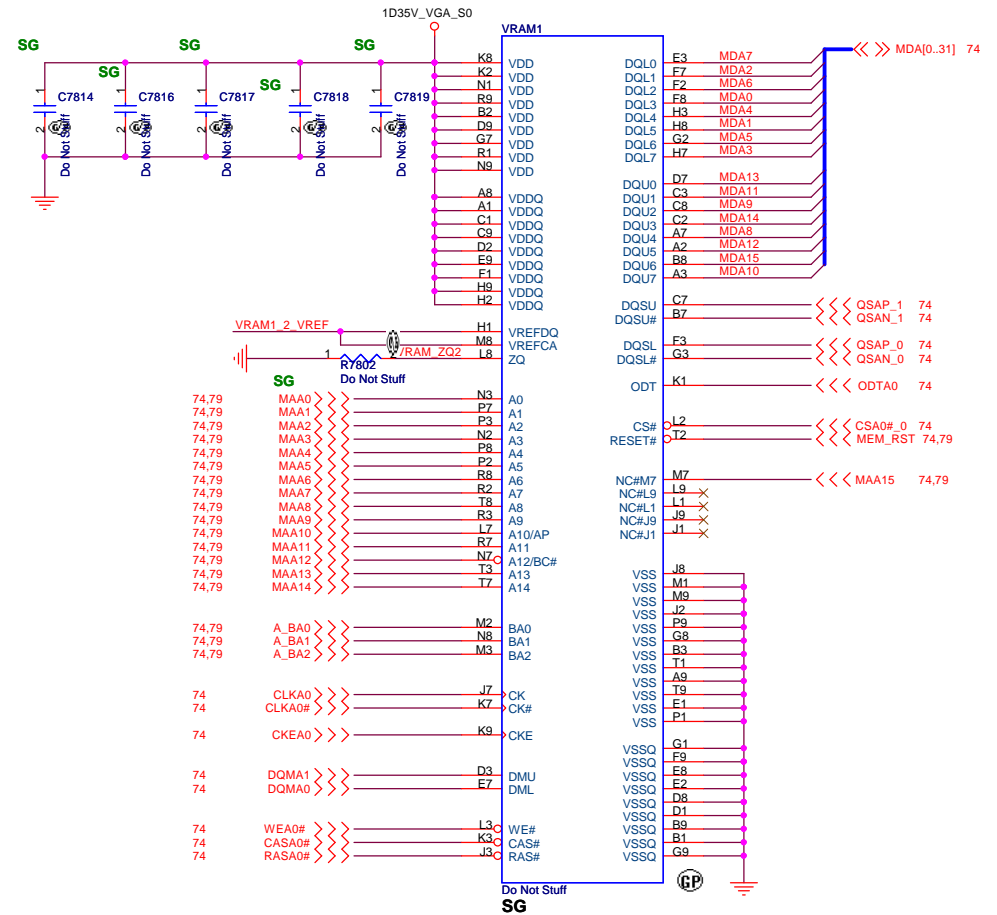
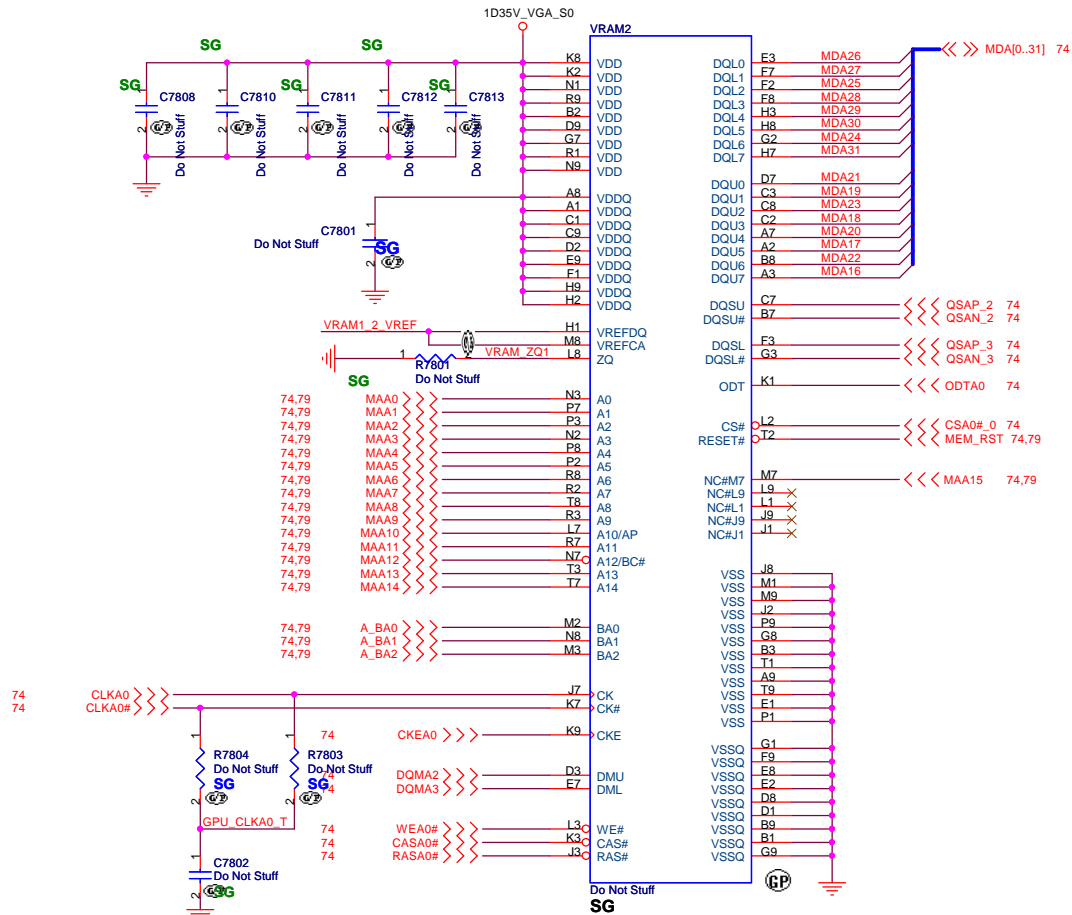


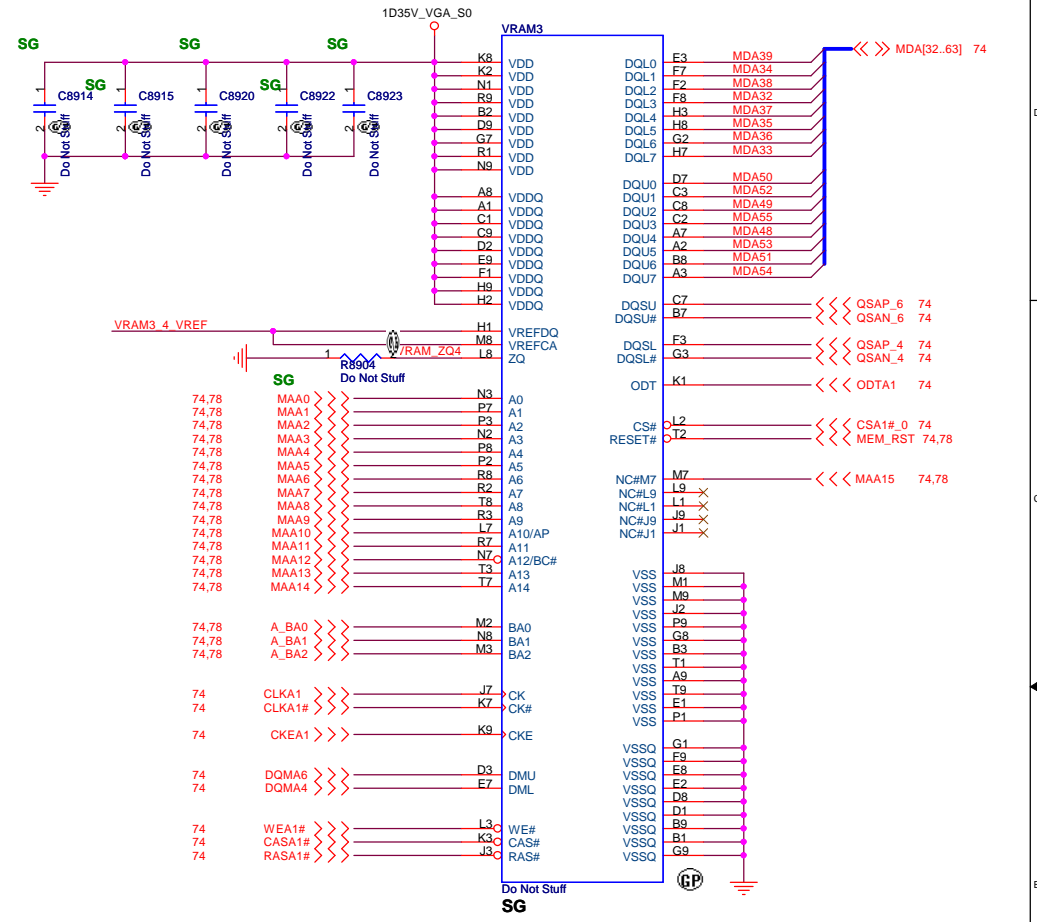
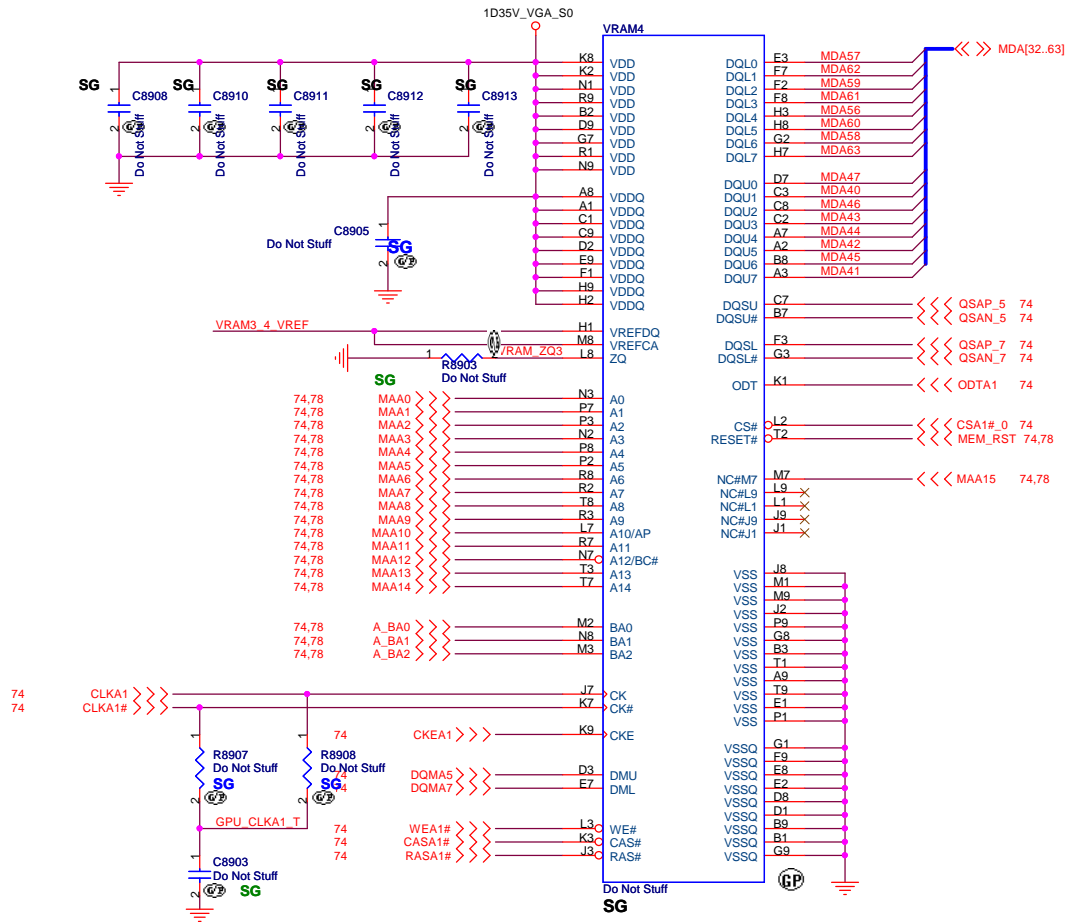
	Bit5,4		Bit3,2,1			
	C	nF	R_pu	K Ohm	R_pd	K Ohm
PS0	C8517	NC	R8521	8.45	R8522	2
PS1	C8519	680	R8517	NC	R8524	4.75
PS2	C8518	680	R8523	NC	R8526	4.75
PS3	C8516	NC	R8527	NC	R8520	4.75





Title			
GPU_POWER/GND			
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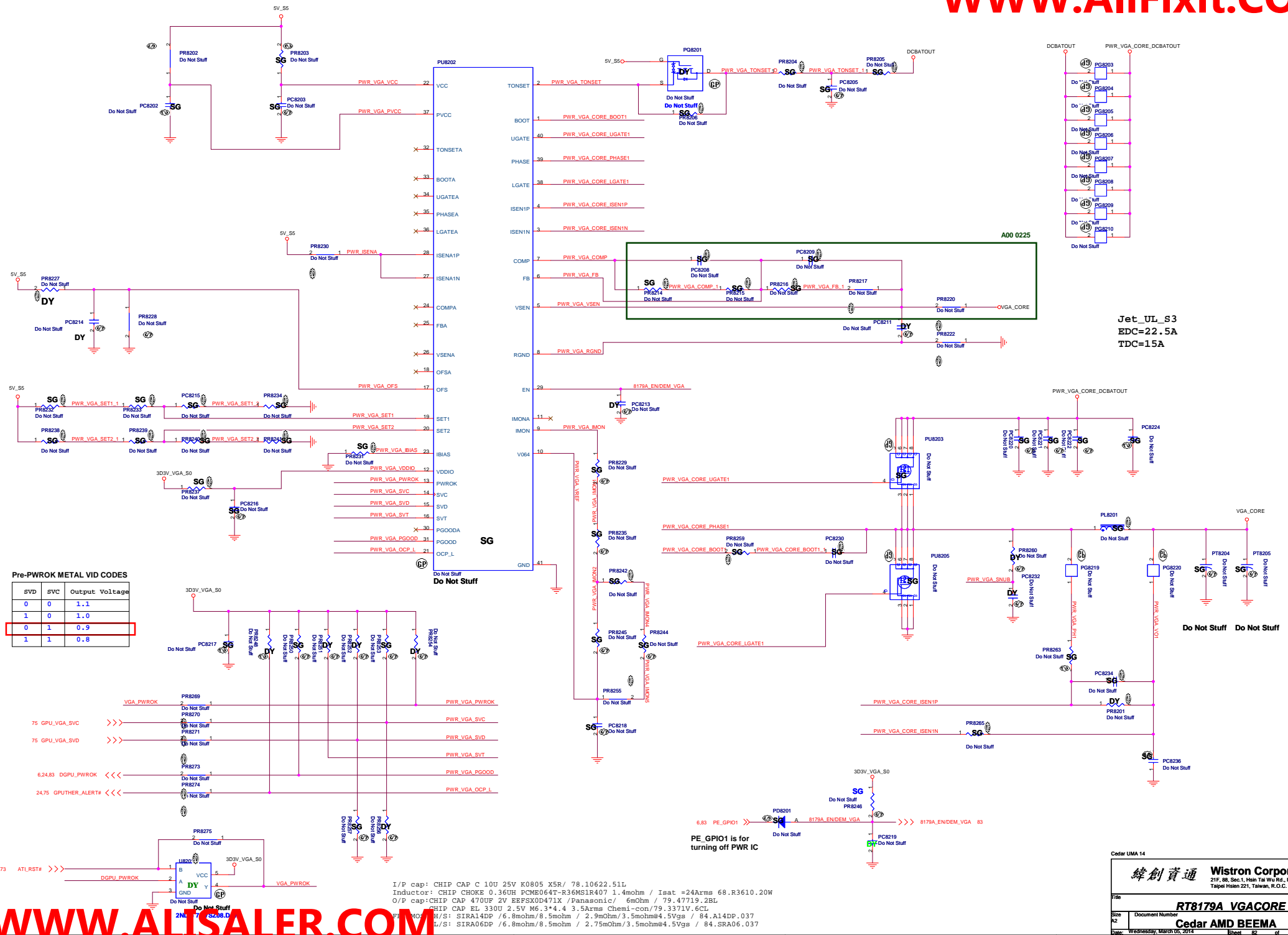
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<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Reserved</div>		
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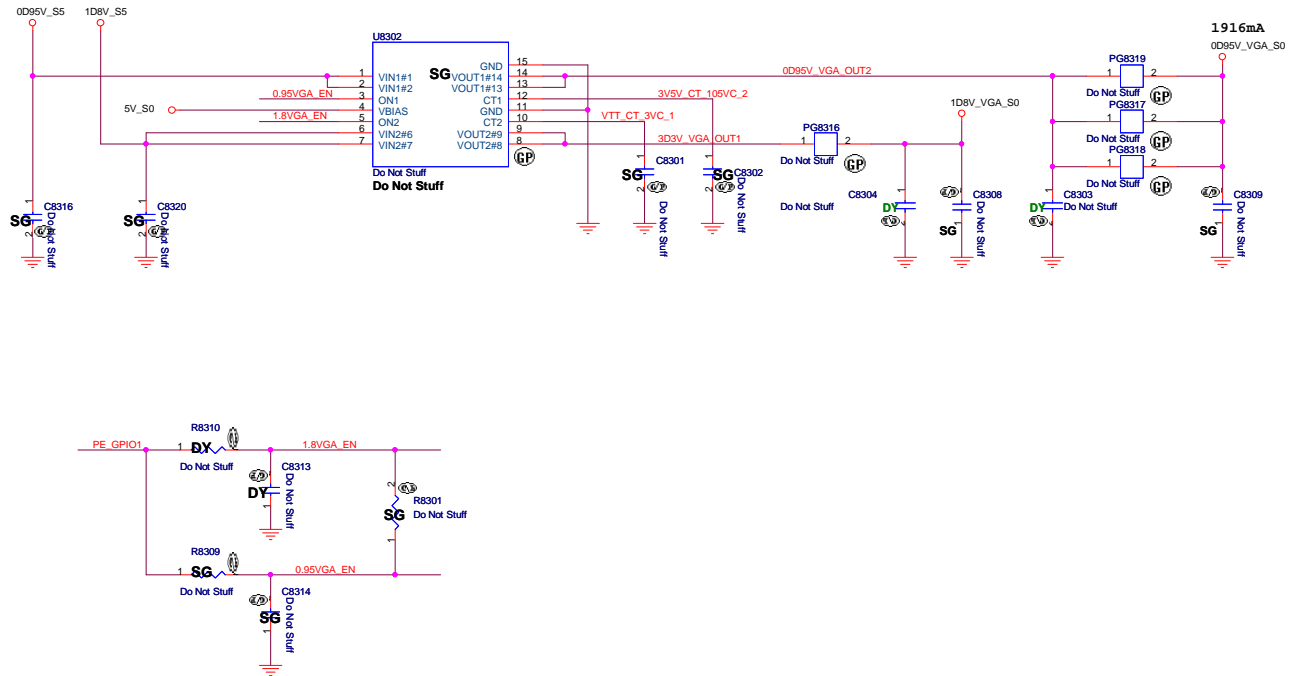
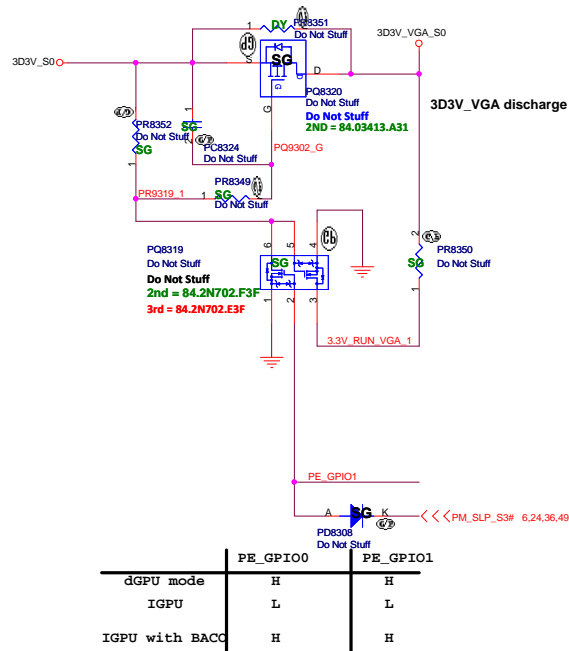
Cedar UMA 14

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Title <div>Reserved</div>		
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# 3D3V\_S0 to 3D3V\_VGA\_S0 Transfer

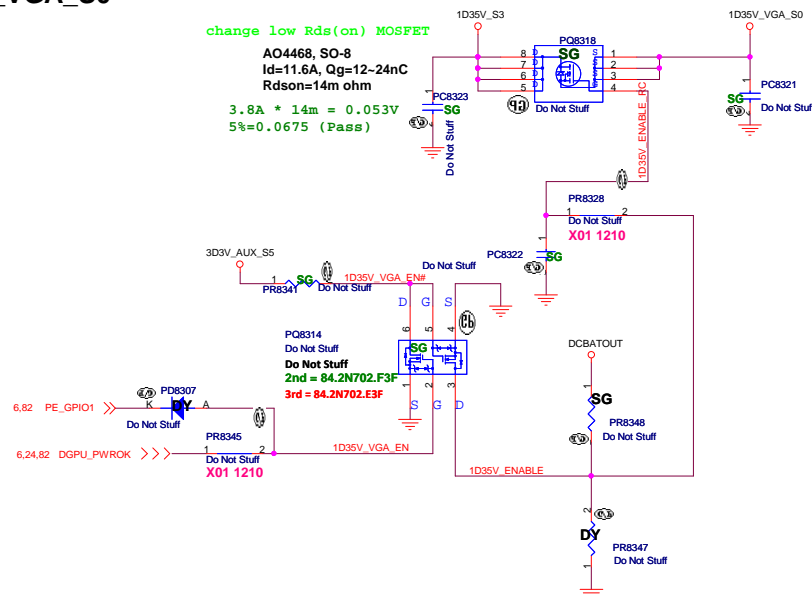
Change DUMMY Reference Name to PX\_BACO



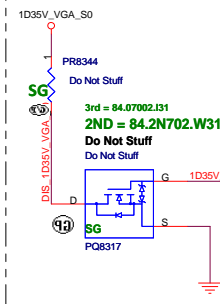
finally rising of 1.8\_VGA\_S0

## 1D5V\_VGA\_S0

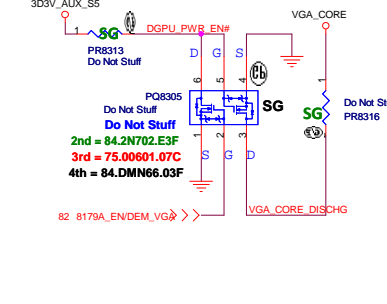
change low Rds(on) MOSFET  
AO4468, SO-8  
Id=11.6A, Qg=12-24nC  
Rdson=14m ohm  
 $3.8A * 14m = 0.053V$   
 $5\% = 0.0675$  (Pass)



### Discharge Circuit



### VGA\_CORE Discharge Circuit



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Title			
DISCRETE VGA POWER			
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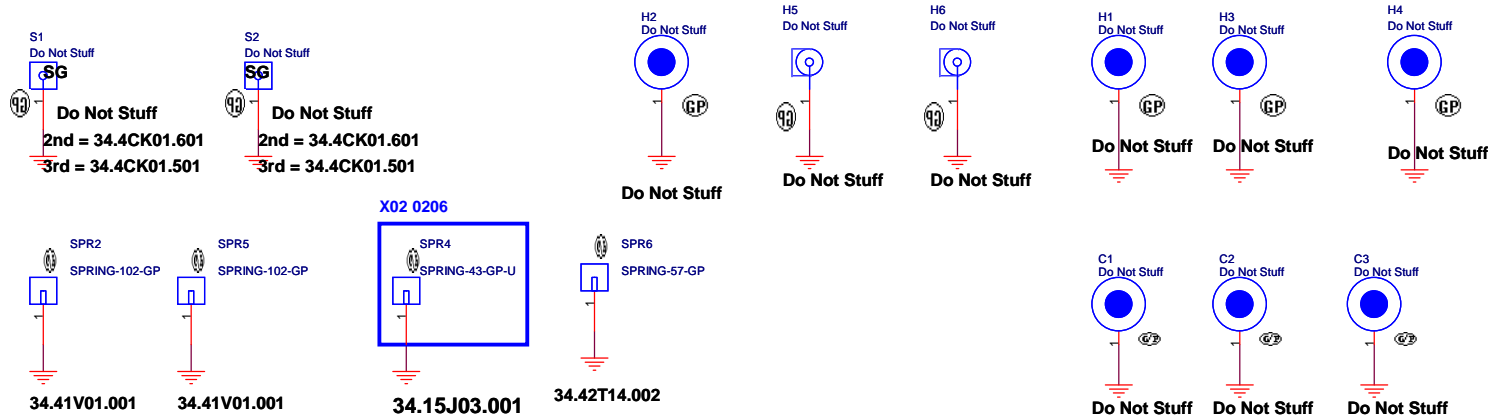
<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>(Reserved)</div>		
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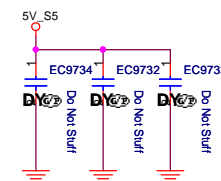
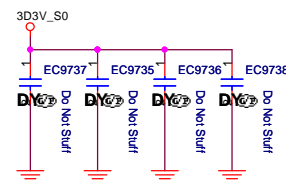
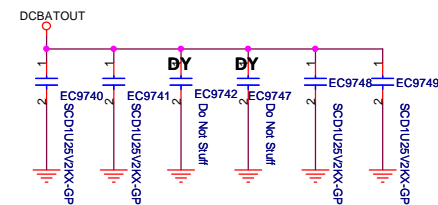
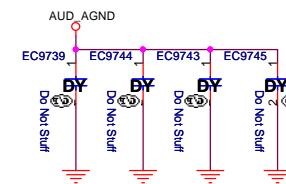
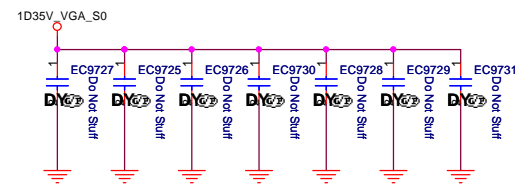
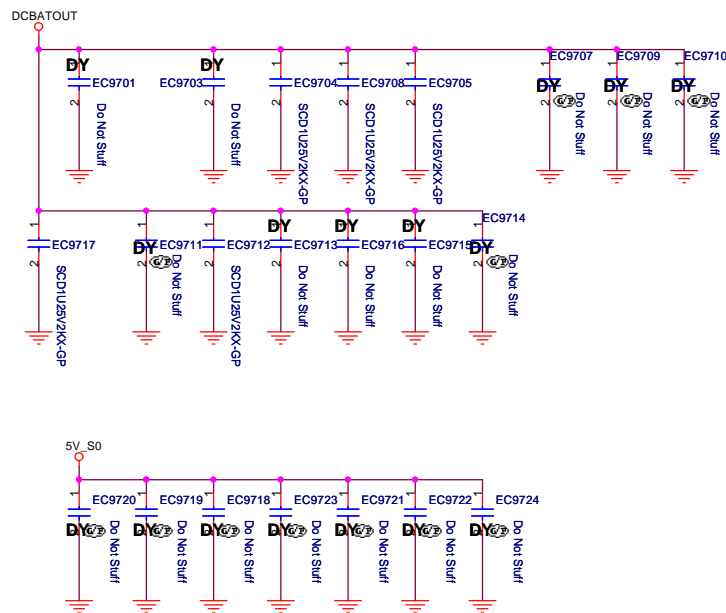
Cedar UMA 14

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Title <div>(Reserved)</div>		
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SSID = Mechanical



SSID = EMI



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Title <div>NFC(Reserved)</div>		
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<div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>			
<div>Title</div>			
<div>TPM/TCM</div>			
<div>Size</div>	<div>Document Number</div>	<div>Rev</div>	
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緯創資通		Wistron Corporation	
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsuehshien, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
Reserved K Series Connector			
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緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
File			
TEST PAD			
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<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>(Reserved)</div>		
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<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
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Cedar UMA 14

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Title <div>(Reserved)</div>		
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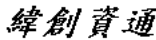
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Title <div>(Reserved)</div>		
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Title			
<b>MCP CPU XDP HDT+</b>			
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D

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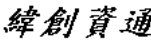
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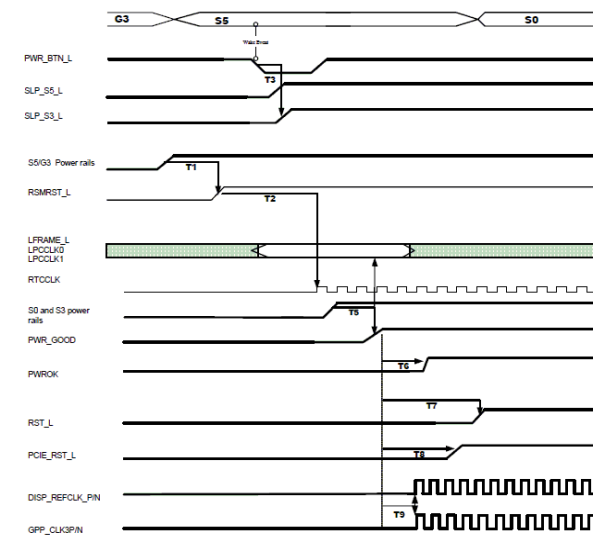
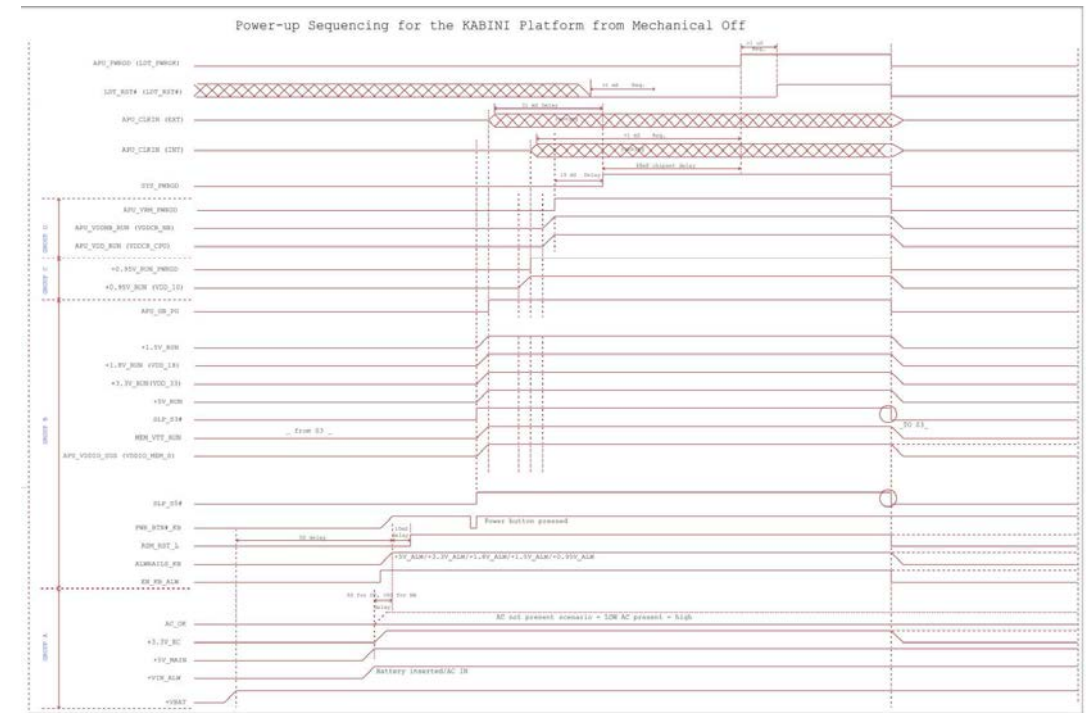
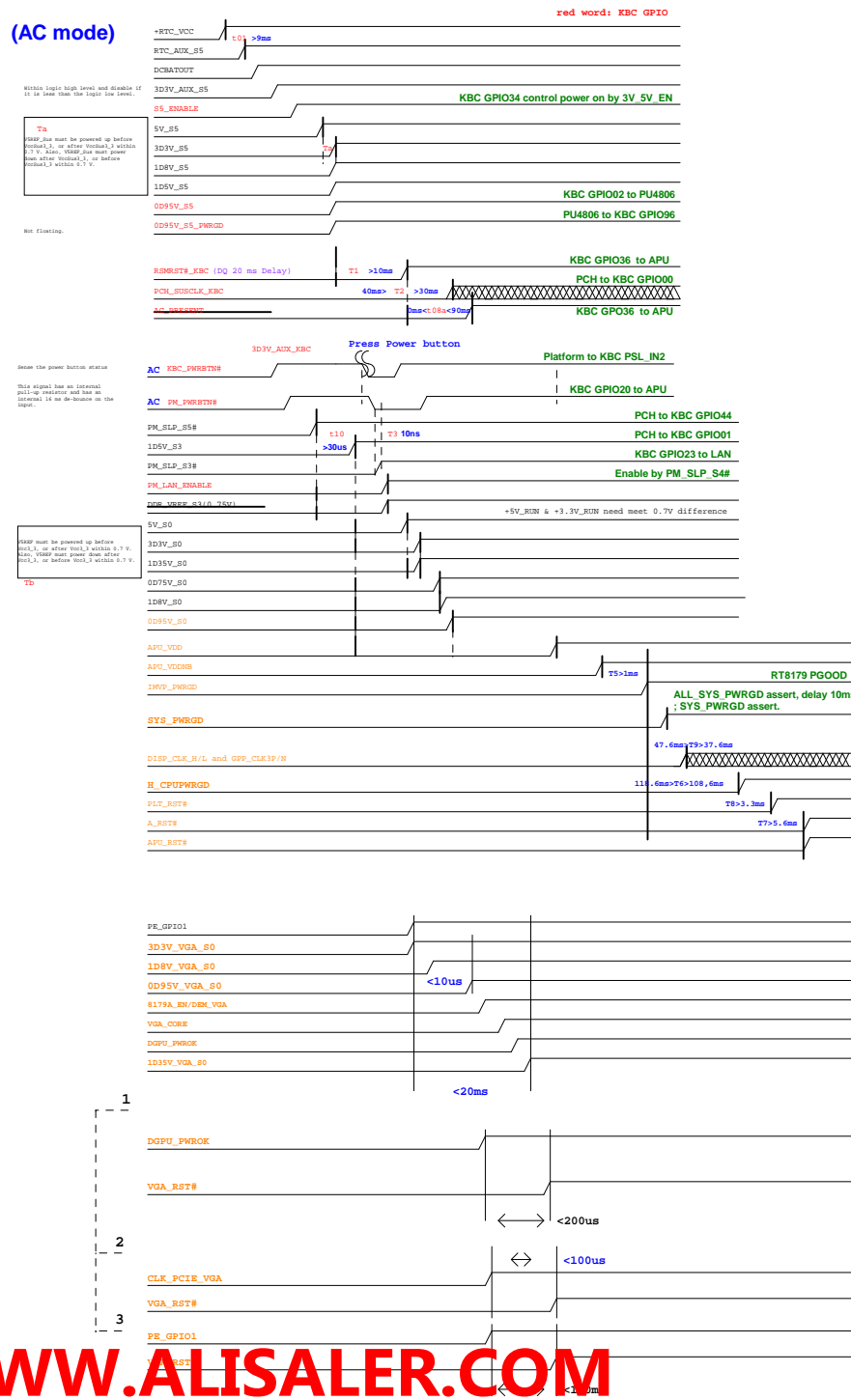
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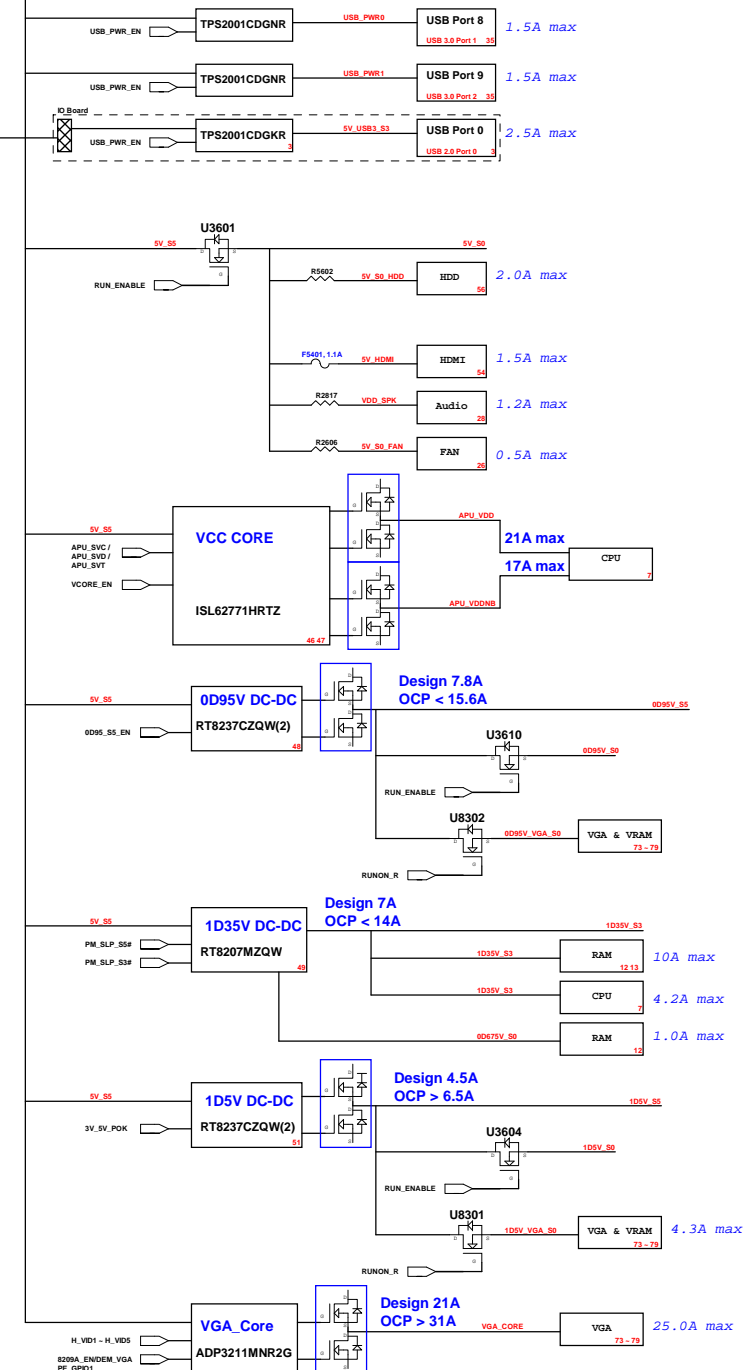
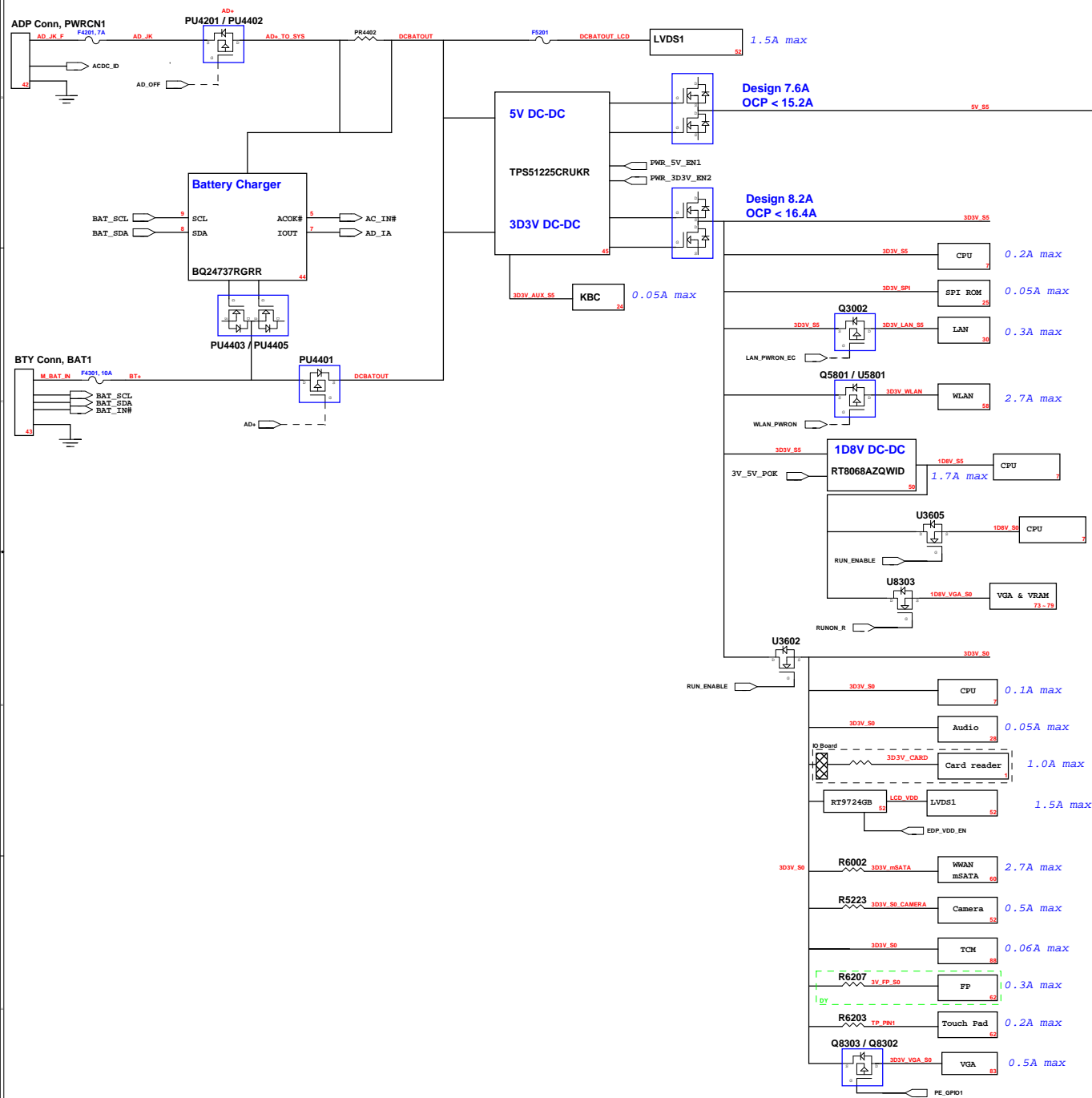
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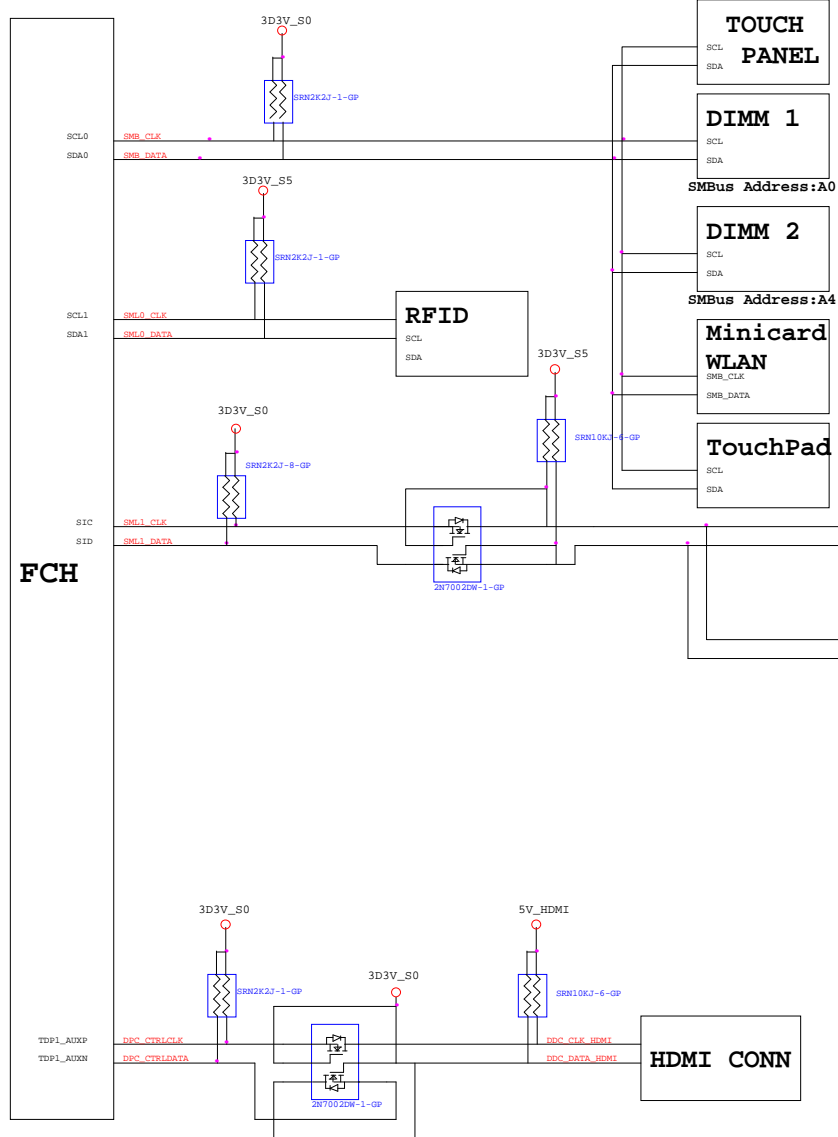
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Change History</b>			
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## Beema Platform Power Sequence

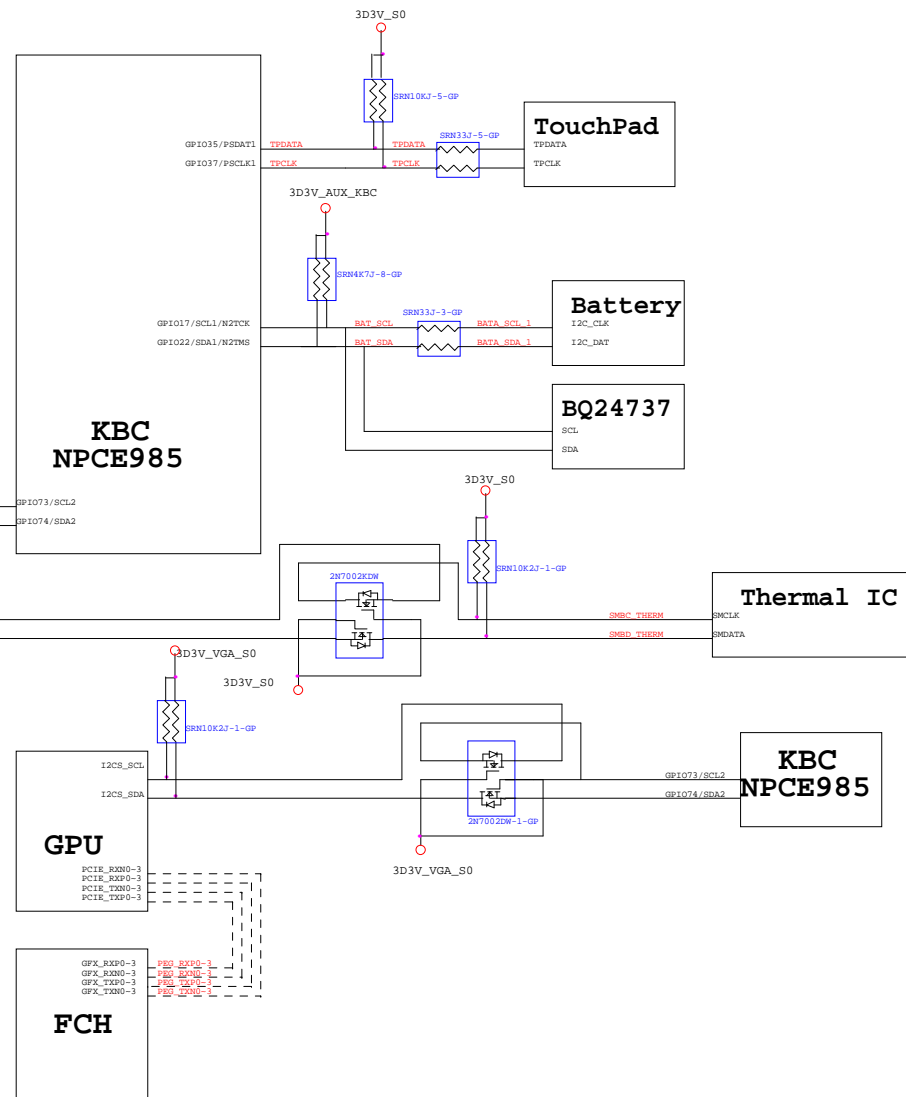




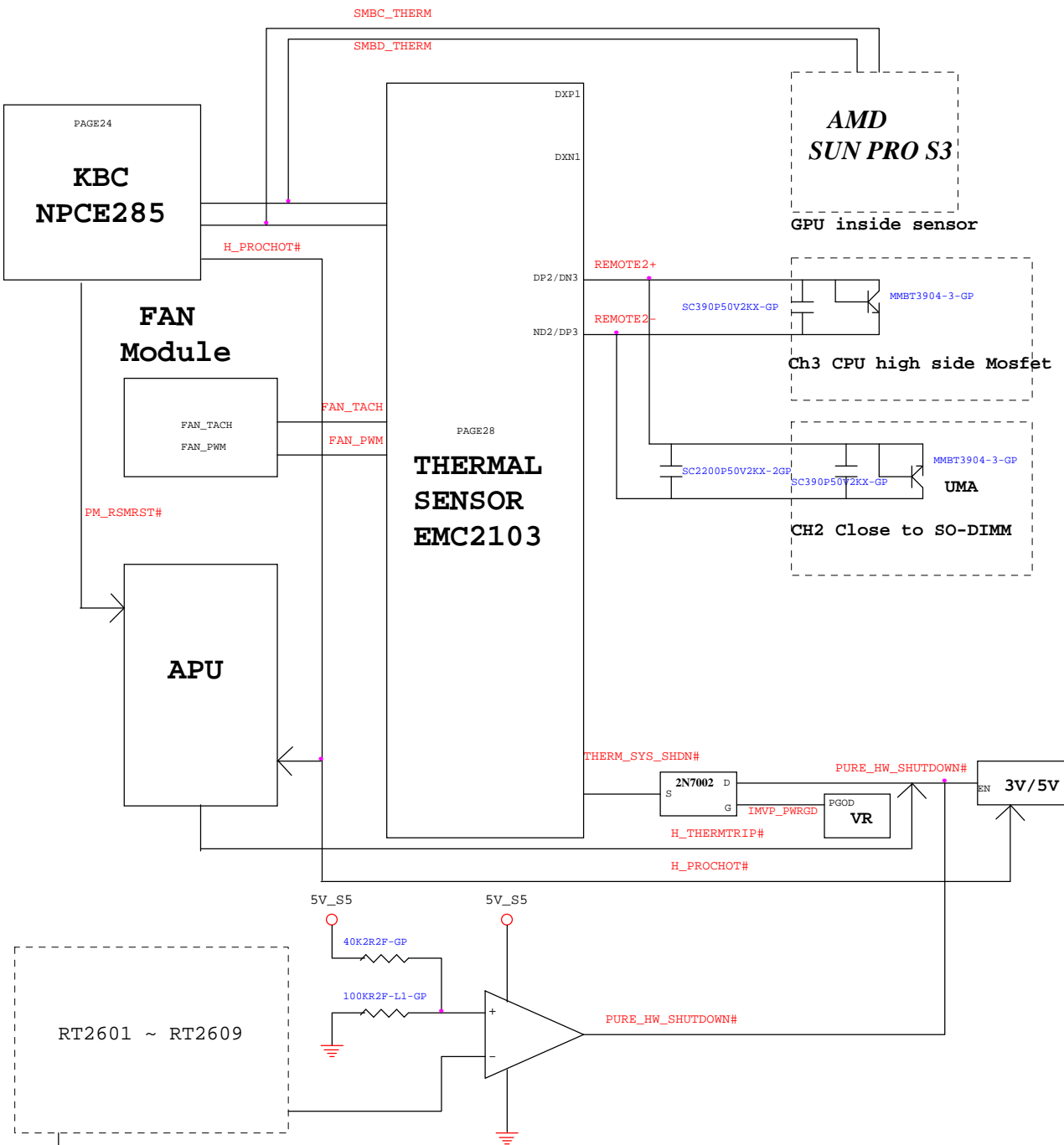
# PCH SMBus Block Diagram



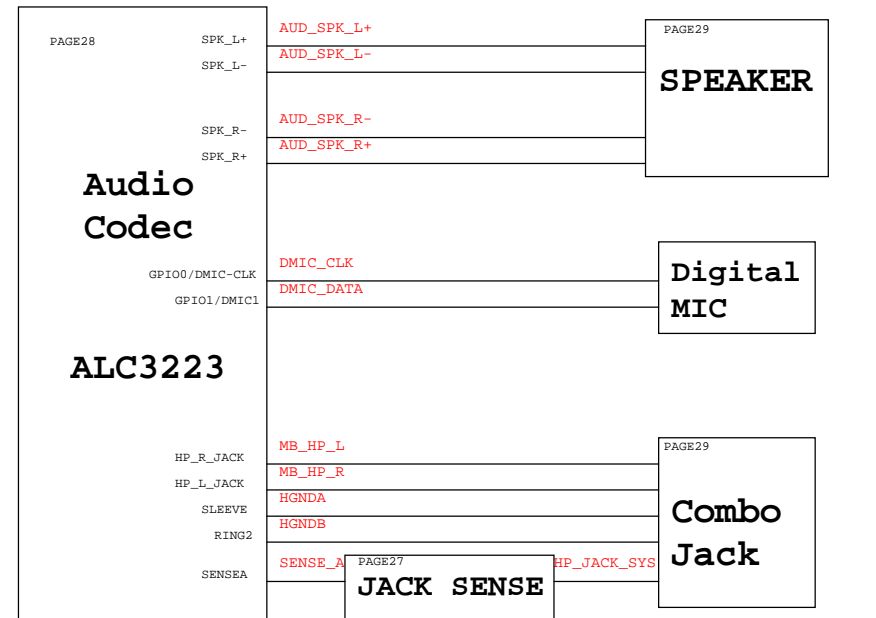
# KBC SMBus Block Diagram



# Thermal Block Diagram



# Audio Block Diagram



	VERSION	DATE	Page	Modify List	OWNER
	X01	2013/12/3	83	R8309 = 15Kohm ,C8301/C8313 = DY,C8302 = 1000pF	
	X01	2013/12/3	43 44	RN4301 to 100ohm, AC_IN# change to Pull-H 3D3V_AUX_S5(PR4434)	
	X01	2013/12/3	27	HDA27 change from ALS3223 to ALC3234	
	X01	2013/12/3	24 25	Swap BATT_WHITE_LED# and EC_BRIGHTNESS. BATT_WHITE_LED# to GPIO13 and EC_BRIGHTNESS to GPIO15. Change R2404 from 10K to 20K ohm for PCB VERSION strap , Del SKT25	
	X01	2013/12/3	52	Reserve 0805 0 ohm R5211 between LCDVDD and LCD1.F5201 change from 69.50007.A31 to 69.60040.001	
	X01	2013/12/3	Power	Change C5205,EC4304,EC4601,PC4409,PC4419,PC4511.PC4518,PC4524,PC4720,PC4722,PC4827,PC4913 to 78.10422.2BL (0.1U 25V K0603 X7R) from 78.10424.2BL (0.1U 50V K0603 X7R).	
	X01	2013/12/3	54 55	Add HDMI SMBUS use 0 ohm DUMMY co-lay ,Add Hsync Vsync 0ohm DUMMY co-lay	
	X01	2013/12/3	29	Change HPMIC1 to 022.10002.0001 from 22.10270.G61 SPK1 change to 20.F1639.004	
	X01	2013/12/3	34 63	Change USB1 to 22.10341.Q21 / Change KBLIT1 to 20.K0800.004	
	X01	2013/12/3	19 26	Change C1904 and C1905 from 10pf to 6.8pf / Q2601 RN2602 DUMMY, RN2601 install	
	X01	2013/12/3	30	R3004 CLK_LAN_REQ0#_R change pull high to 3D3V_S0	
	X01	2013/12/3	EMI	DMIC_CLK mount R2716 100ohm resistance,Mount EC9749,Mount EC4304	
	X01	2013/12/3	58	CARD_WLAN_OUT# and CARD_WPAN_OUT# modify to TP change WLAN1 to 62.10043.I81	
	X01	2013/12/3	42 51	DCIN1 change to 20.F1783.007,Del 1D5V_S5 circuit	
	X01	2013/12/4	24 34 35	R2447 change to 63.10334.1DL,Del U3502 and U3501,swap the net U3403.1 and U3403.3	
	X01	2013/12/5	42 46 24 26	Del AFTP3804 AFTP3807, Modify AFTP6241 Add AFTP6242,Change R2447 to 1K , R2622 change to 24.3K	
	X01	2013/12/6	24	R2411 DY D2401 install	
	X01	2013/12/9	31 47 82	RJ45 connector change to 022.10001.0551, PT4701 /PT4704/PT8204 change to 79.3371V.6CL	
	X01	2013/12/10	EMI	Mount EC4303 and change to 0.1u Mount EC9705 EC9748 EC9717 EC9740 EC9741 EC9712 EC9704 EC9708 and change to 0.1u Mount R5415、R5417、R5416、R5414 150ohm resistance Mount TR3401、TR3404、TR6301(69.10103.041、69.10080.011) Mount TR5208、TR5209(69.10103.041、69.10080.011) Mount EC2705、EC2703、EC9739、EC9743、EC9744 0.1u cap Mount SPR2、SPR5、SPR6	
	X01	2013/12/10	0 ohm	change 0 ohm to short pad	
	X01	2013/12/10	54 55	R5501/R5502 change to 33 ohm / Del D5402	
	X01	2013/12/10	24 52 62	R2411 Install D2401 DUMMY ,R5207 BOM control ,BOM control DVC50 to Janus	
	X01	2013/12/12	46 86 62	PR4609 change to 44.2K (64.44225.6DL) from short pad, EMI:Add SPR6(34.42T14.002),KBLIT DUMMY	
	X01	2013/12/16	55 Power	Del CRT circuit / Modify power schematic BOM	
	X01	2013/12/18	Power	PR8214 change to 499K (64.49935.6DL) / PR8215 change to 9.76K (64.97615.6DL)	

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緯創資通

**Wistron Corporation**  
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 Taipei Hsien 221, Taiwan, R.O.C.

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Change List

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	VERSION	DATE	Page	Modify List	OWNER				
	X02	2014/01/21	48	Change PR4823 to 26.1K. The voltage about 0.97V					
	X02	2014/01/21	83	R8310 change 15Kohm /C8313 change 0.1uF /C8301 change 470pF Add R8301 for power sequence					
	X02	2014/01/27	12,46	EMC request:change EC4601,C1217,C1225,C1214 to 0.1u					
	X02	2014/01/27		Change 0 ohm to short pad					
	X02	2014/01/27	6	DGPU_PRESENT# pull hi to 3D3V_S0					
	X02	2014/01/28	power	1. PD4201 change 1st source to 83.P6SEM.AAG and 2nd source to 83.P6SEM.DAG . 2. PC4202 PC4409 PC4419 PC4519 PC4524 PC4511 PC4513 PC4518 PC4734 PC4720 PC4722 PC4736 PC4833 PC4827 PC4919 PC4913 PC8230 change to 78.10424.2BL. 3. PC4201 change to 78.10594.41L. 4. PC4916,PC4917 change to 78.10610.5BL. 5. PC4408 change to 78.47522.51L (4.7U 25V K0805 X5R). 6. PC4425 change to 78.10324.2FL (0.01U 50V K0402 X7R). 7. PC4512 change to 78.47522.51L (4.7U 25V K0805 X5R). 8. Delete PC4814/PC4714. 9. Dummy PC4718/PC4912/PC4920/PC4204/PC4205/ PC4426/PC4416/PC4830 10.PC4828 change to 78.47522.51L (4.7U 25V K0805 X5R). 11.PC4909 and PC4911 change to 78.47522.51L (4.7U 25V K0805 X5R).					
	X02	2014/01/28	31	change XF3101 and XF3102 to 68.68167.30D and Swap net					
	X02	2014/02/06	06 19	Change RN1901 R1901 from short pad to 0 ohm Change RN604 to 66.10336.08L					
	X02	2014/02/06	86	Change SPR4 P/N to 34.15J03.001					
	X02	2014/02/07	26	THM26 DUMMY, Add R2602 for VD_OUT1# connect PURE_HW_SHUTDOWN#					
	A00	2014/02/25		Change PR4911 PR4649 R3016 R6209 R1901 RN5404 RN1901 to short pad					
	A00	2014/02/25	82	Modify schematic PWR_VGA_COMP connecte to PWR_VGA_FB					
	A00	2014/02/25	24	PCB VERSION A/D(PIN98) R2404 change to 64.64925.6DL					
	A00	2014/02/25	54	Install D5401 RN5401 Q5402, Dummy RN5404					
WWW.ALISALER.COM					<div> <div>Cedar UMA 14</div> <div> <div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div> </div> <div> <div>Change List</div> <div> <div>Size A3</div> <div>Document Number</div> <div>Rev A00</div> </div> <div> <div>Date: Wednesday, March 05, 2014</div> <div>Sheet 104 of 104</div> </div> </div> </div>				